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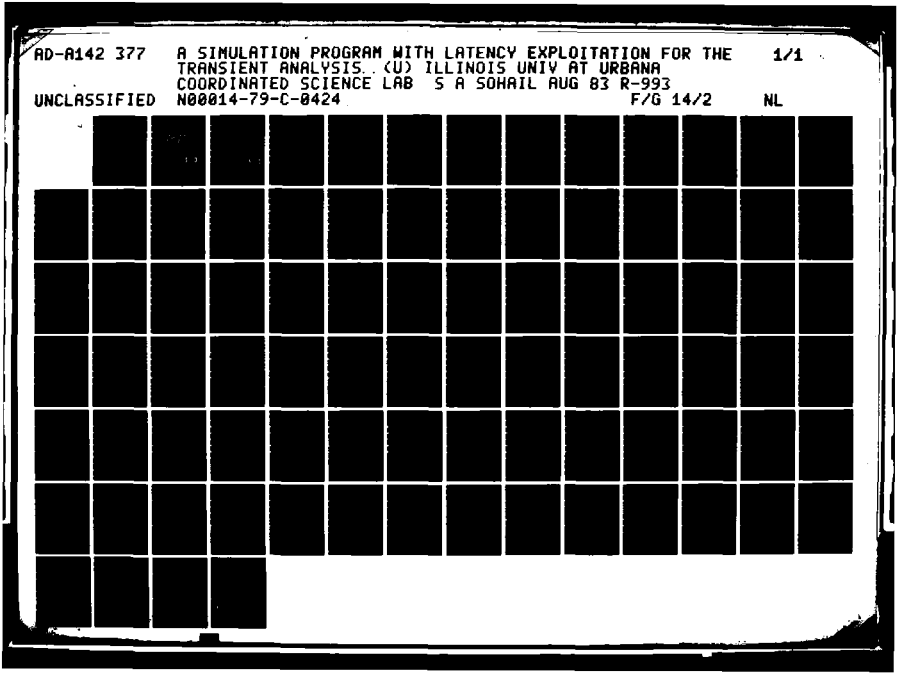

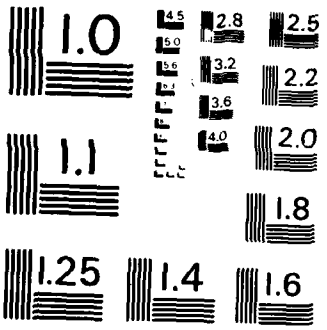

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A SIMULATION PROGRAM WITH LATENCY EXPLOITATION FOR THE TRANSIENT ANALYSIS OF DIGITAL CIRCUITS

SAJID AHMED SOHAIL

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This report examines the efficiency that can be obtained in the simulation of large digital integrated circuits with the implementation of latency, that is, inactive gates in a given time interval are bypassed in the simulation. In particular the latency criterion in the program SLATE is studied, and a user's guide to SLATE is included.

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A SIMULATION PROGRAM WITH LATENCY EXPLOITATION FOR THE TRANSIENT ANALYSIS OF DIGITAL CIRCUITS

BY

SAJID AHMED SOHAIL

B.S., University of Illinois, 1982

THESIS

Submitted in partial fulfillment of the requirements
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in the Graduate College of the
University of Illinois at Urbana-Champaign, 1983

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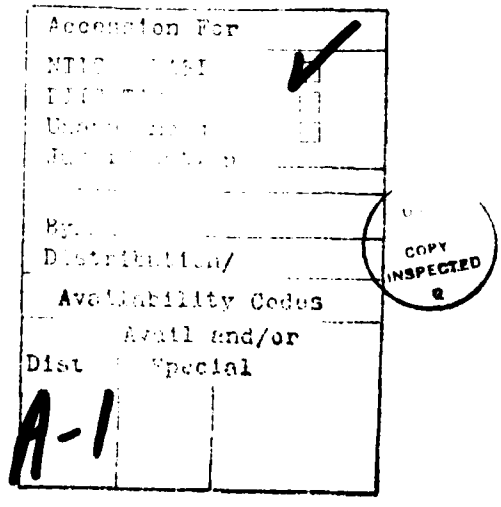

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CHAPTER 1

INTRODUCTION

The challenge of simulating integrated circuits (ICs) is becoming more formidable with the rapidly increasing number of devices on a chip. The conventional circuit simulation programs [1-4] use a prohibitive amount of computing resources for today's large scale integrated (LSI) circuits. These simulators do not exploit the two inherent properties of digital ICs, namely, repetitiveness and latency. SLATE (a Simulator with Latency and Tearing) is a simulation program which attacks the problem of simulating LSI circuits by exploiting the above stated properties of digital circuits. SLATE was orignally developed from SPICE2 [1] by Ping Yang of The Coordinated Science Laboratory and the Department of Electrical Engineering at The University of Illinois [5].

It was the goal of this research to benchmark the program SLATE against SPICE2 (version G.1)[1], and show by example circuits that the latency exploitation approach in SLATE does in fact save computer time as the size of the circuits simulated increases. In order to do so, a VAX11/780 UNIX version of SLATE was created in the initial stages of this research. This version of SLATE also includes a new charge conserving MOSFET model with subthreshold conduction and short channel effects [6,7].

Chapter 2 of this thesis describes in detail the new MOSFET model implemented in SLATE and the modified Gummel-Poon [8] model for bipolar

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[1] Version G.5A was not used due to convergence problems for some of the example circuits we simulated.

transistors. Chapter 3 describes the latency scheme in SLATE and the experimental results achieved by exploiting latency in example circuits. Finally, the Appendix lists the user's guide to SLATE, with the example circuits at the end.

CHAPTER 2

MOSFET AND BIPOLAR DEVICE MODELS IN SLATE

VLSI circuits impose several very important restrictions on the device models in circuit simulators. The device models should be computationally efficient, sufficiently accurate, memory requirements should not be too high, and convergence probability should be high. SLATE incorporates a MOSFET model based on a quasi-physical set of equations with a parameter vector which can be extracted from measured data. The model includes above threshold and subthreshold components of current, short-channel effects, and a charge-conserving capacitor model [6], [7]. The model is computationally very efficient due to its simplicity, and its convergence properties are better than Meyer's model [9] due to smooth transitions of current and charge among different regions.

The bipolar junction transistor model in SLATE is an adaption of the integral charge control model of Gummel and Poon [8]. The model reduces to the simpler Eber-Moll model if the additional Gummel-Poon parameters are not specified.

2.1. MOSFET Model

The current-voltage characteristics and the four terminal nonreciprocal capacitor characteristics of the MOSFET device are basic components of the model. Figure 2.1 shows the MOSFET model in SLATE.

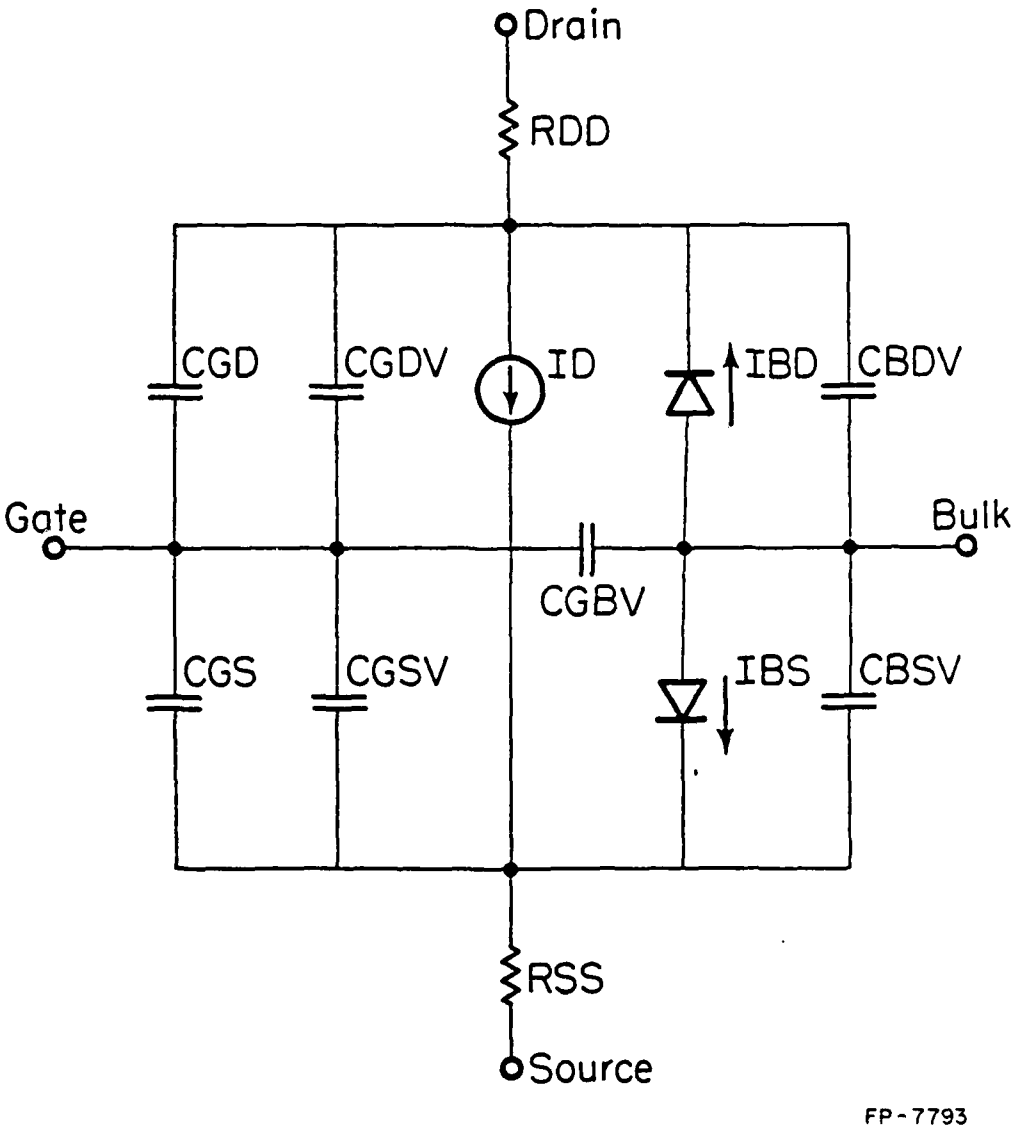


Figure 2.1 MOSFET Model

2.1.1. DC model

The dc model in SLATE is based on a quasi-physical current model which includes subthreshold and above threshold regions of operation. The model equations are described below.

Threshold voltage equation:

The threshold voltage equation for a long channel MOSFET is modified to represent the bulk charge Q_B sharing between the gate, drain and source. The effect of this charge sharing is to reduce the threshold voltage [10].

$$V_t = V_{to} + BE*((2\phi_f - V_{bs})^{1/2} - (2\phi_f)^{1/2}) - DE*((2\phi_f + V_{ds} - V_{bs})^{1/2} - (2\phi_f)^{1/2})*(2\phi_f - V_{bs})^{1/2} \quad (2.1)$$

where

$$BE = \frac{(2q\varepsilon_{si}Na)^{1/2}}{Cox}$$

$$V_{to} = V_{FB} + 2\phi_f + BE*(2\phi_f)^{1/2} \quad (2.2)$$

$$V_{FB} = \phi_{MS} - \frac{Q_{ss}}{C_{ox}} \quad (2.3)$$

BE is the body effect term for long channel device, and DE, the drain effect term, represents the drain induced barrier lowering. The parameters BE, DE, and V_{to} can be extracted from the measured I-V data. It may be noted that for small geometry devices, BE and DE will be dependent on the length and width of the device. The width dependence is due to the oxide encroachment which is common in today's processes.

This effect has been theoretically studied in [11] and [12], and experimentally verified in [7].

Drain current equations:

The drain current expressions in SLATE take into account the lateral electric field effect in short channel devices. This lateral field modifies the channel quasi-fermi level Vy. The unique attribute of this model is the factor α_x which is found to be adequate in representing the effects of the lateral electric field [7].

$$\alpha_x = \alpha + \gamma * V_{gst} \qquad (2.4$$

where

$$V_{gst} = V_{gs} - V_t$$

$$\alpha = KP1inear/KPsaturation$$

The parameter γ is a short channel parameter, representing the velocity saturation effect.

The drain to source current without the subthreshold component in the three regions of operation is given by:

Cutoff region: $V_{gst} < 0$

$ID = 0$

Linear region: $V_{dsat} > V_{ds}$

$$ID = \frac{\alpha_x * KP * (W-WR) * (2 * V_{gst} * V_{ds} - \alpha_x * V_{ds}^2)}{(L - TLD - LR) * (1 + \partial * V_{gst})} \qquad (2.5a)$$

Saturation region: $V_{dsat} < V_{ds}$

$$ID = \frac{KP(W - WR)V_{gst}^2 * (1 + \lambda(\alpha/\alpha_x)^2 (V_{ds} - V_{dsat}))}{(L - TLD - LR)(1 + \partial * V_{gst})} \qquad (2.5b)$$

where

$$V_{dsat} = \frac{V_{gst}}{\alpha_x}$$

$$KP = \frac{\mu_n C_{ox}}{2}$$

In the above equations TLD is the total lateral diffusion (sum of the source and drain lateral diffusions). LR and WR are the mask tolerance length reduction and width reduction factor due to the oxide encroachment. The parameters ∂ (THETA) and λ are the mobility variation factor and the channel length modulation factor which is roughly proportional to 1/(L - TLD), respectively. The parameters α, γ, ∂, and λ are a part of the parameter vector which can be extracted from the measured data. See Table 2.1 for an example parameter vector for L = 1.5μm and W = 5μm device [7].

The subthreshold component of the current is added to the device drain current in all three regions if the user specified parameter KPS is not zero. The simplified expression for the subthreshold current, derived by solving the Poisson equation for effective Q_B, is given below [7].

For $V_{gs} > V_t$

$$ID_{sub} = \frac{KPS*(W - WR)}{(L - TLD - LR)}*(1 - e^{-NG\beta V_{ds}}) \qquad (2.6)$$

For $V_t > V_{gs} \geq V_{bs} + V_{FB}$

$$ID_{sub} = \frac{KPS*(W - WR)}{(L - TLD - LR)}*(1 - e^{-NG\beta V_{ds}})*e^{NG\beta(V_{bs} + U_s - 2\phi_f)} \qquad (2.7)$$

where

$$\beta = Q/K*T$$

$$KPS = \frac{2^{1/2}\mu_n \varepsilon_{si}}{NG\beta^2 LD}$$

$$U_s = V_{gs} - V_{bs} - V_{FB} + \frac{BET^2}{2}(1 - (1 + 4(V_{gs} - V_{FB} - V_{bs})/BET)^{1/2})$$

$$BET = BE - DE((2\phi_f - V_{ds} - V_{bs})^{1/2} - (\phi_f)^{1/2})$$

where LD is the extrinsic Debye length and NG is a correction factor used to represent the approximations made in deriving the above current equations, and the uncertainty in the exact device temperature. KPS and NG are also extracted from the measured data, see Table 2.1.

Table 2.1 Extracted Parameter Vector

Parameter	Value
V_{to}	0.591212E+00
BE	0.637995E+00
DE	0.331291E-01
α	0.105286E+01
∂	0.236235E+00
λ	0.109119E+00
γ	0.119909E+00
KPS	0.973771E-06
NG	0.835092E+00

2.1.2. Transient model

Extrinsic region capacitances:

The MOSFET device can be partitioned into extrinsic and intrinsic regions as shown in Figure 2.2. The extrinsic region capacitances are modelled by fixed overlap, fringing and lateral diffusion capacitances plus drain and source p-n junction capacitances and sidewall capacitances.

Overlap capacitances:

$$C_{gs} = C_{ox}*(W - WR)*(LGOS + .5TLD) \quad (2.8)$$

$$C_{gd} = C_{ox}*(W - WR)*(LGOD + .5TLD) \quad (2.9)$$

where LGOS and LGOD are gate to source and gate to drain overlaps, respectively.

Fringing capacitance:

The fringing capacitances becomes important if the gate electrode thickness is comparable to the gate oxide thickness. SLATE includes a fringing capacitance model which models the finite gate electrode thickness effect.

$$CFR = \frac{W*\varepsilon_{ox}}{\pi} *((x + 1/x)\ln((1 + x)(1 - x)) + 2\ln(.25(1/x - x))) \quad (2.10)$$

where

$$x = \frac{T_{ox}}{(T_{ox} + T_{poly})}$$

where T_{ox} is the gate oxide thickness and T_{poly} is the gate electrode

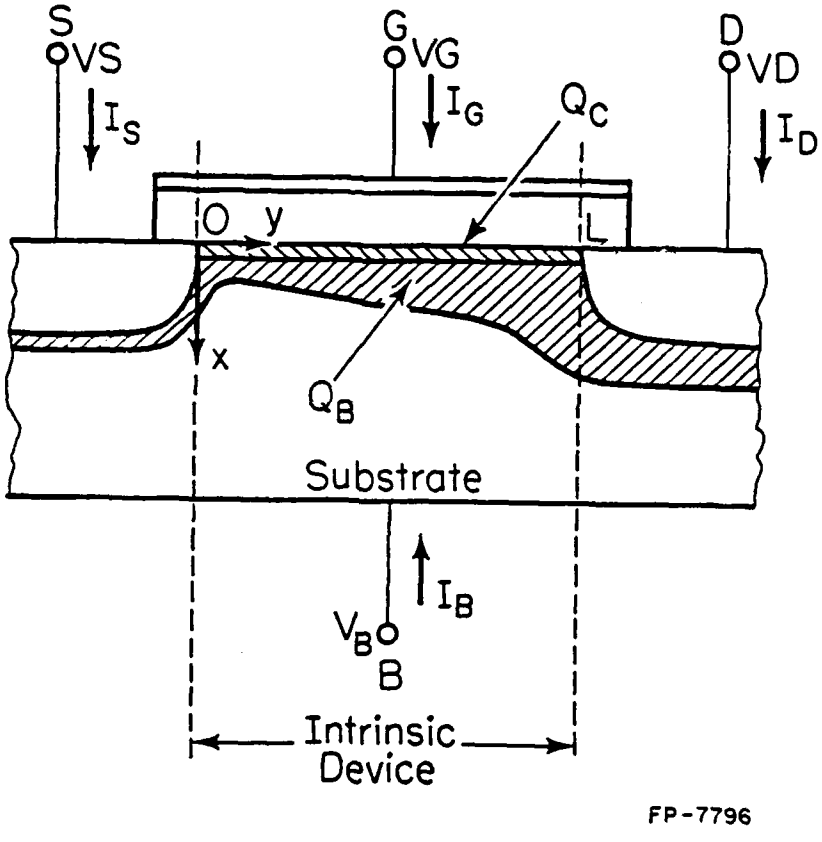


Figure 2.2 MOSFET Device

thickness. CFR is added to gate-source and gate-drain capacitances.

Junction capacitances:

The p-n junction capacitances are modeled by bottom junction capacitances and sidewall junction capacitances.

Bottom capacitances:

$$C_{bs} = \frac{AS*KPN}{(2\phi_f)^{1/2}(1 - V_{bs}/2\phi_f)^M} \tag{2.11}$$

$$C_{bd} = \frac{AD*KPN}{(2\phi_f)^{1/2}(1 - V_{bd}/2\phi_f)^M} \tag{2.12}$$

Sidewall capacitances:

$$C_{bs} = \frac{ASS*KPN}{(2\phi_{fs})^{1/2}(1 - V_{bs}/2\phi_{fs})^{MS}} *(NS/N)^{1/2} \tag{2.13}$$

$$C_{bd} = \frac{ADS*KPN}{(2\phi_{fs})^{1/2}(1 - V_{bd}/2\phi_{fs})^{MS}} *(NS/N)^{1/2} \tag{2.14}$$

where

$$KPN = \left(\frac{q\varepsilon_{si}Na}{2}\right)^{1/2}$$

and is a constant which models the zero-bias junction capacitance per unit area. AS and AD are source and drain window areas and ASS and ASD are sidewall areas. NS is channel stop impurity concentration and N is bulk concentration.

Intrinsic region capacitances:

The intrinsic MOSFET device in SLATE is modeled by a charge conserving capacitance model recently published in [6]. The model

eliminates the problem of charge nonconservation which occurs in the Meyers model [9]. The model uses analytic charge equations in each region of operation instead of capacitance equations and insures the continuity of charges throughout different regions. The unique feature of the model is the partitioning of the channel charge into drain and source components by using self-consistent boundary conditions. This was not done in the models previously proposed [13], [14].

The charge model equations in the linear and saturation regions are derived from the dc current model. Whereas, the equations in the accumulation and subthreshold regions are derived from solving one dimensional Poisson equations [15], [16]. Two simplifying assumptions made in deriving the equations are (i) the omission of any mobile charge after pinch-off, and (ii) the omission of drain depletion charges.

Let q_g, q_c, and q_b represent the charge densities per unit area on the gate, in the channel, and in the substrate depletion layer. The charge equations in different regions are as follows.

Linear region: $V_{gs} \geq V_{gsat}$

$$q_g = C_{ox}(V_{gs} - V_{FB} - 2\phi_f - Vy) \tag{2.15}$$

$$q_c = -C_{ox}(V_{gs} - V_t - \alpha_x Vy) \tag{2.16}$$

$$q_b = -C_{ox}(V_t - V_{FB} - 2\phi_f - (1- \alpha_x)Vy) \tag{2.17}$$

where Vy is the quasi-fermi potential for electrons and is defined

with respect to the source.

$$V_{gsat} = V_t + \alpha_x V_{ds}$$

To obtain the charge equations we would have to integrate equations (2.15), (2.16), and (2.17) over the width and length of the channel in the linear region; therefore,

$$Q_g = W\int_0^L q_g \, dy \tag{2.18}$$

Substituting for q_g we obtain

$$Q_g = W\int_0^L C_{ox}(V_{gs} - V_{FB} - 2\phi_f - V_y) \, dy \tag{2.19}$$

All the terms in equation (2.19), except for Vy, are assumed to be independent of the channel length; therefore, we need to evaluate,

$$\int_0^L Vy \, dy = \int_0^{V_{ds}} Vy \, dVy \, \frac{dy}{dVy} \tag{2.20}$$

We also know that along the channel

$$ID = W\mu_n C_{ox}(V_{gs} - V_t - \alpha_x Vy)\frac{dVy}{dy} \tag{2.21}$$

Substituting the expression for ID in the linear region, we get

$$\frac{dy}{dVy} = \frac{L(V_{gs} - V_t - \alpha_x Vy)}{(V_{gs} - V_t)V_{ds} - 0.5\alpha_x V_{ds}^2} \tag{2.22}$$

Integrating equation (2.22) from 0 to V_{ds} we get

$$\int_0^{V_{ds}} Vy \frac{dy}{dVy} dVy = L*(0.5V_{ds} - \alpha_x V_{ds}^2/12(V_{gs} - V_t - 0.5\alpha_x V_{ds}))$$

Substituting the above expression in equation (2.19) for Q_g and similarly for Q_b and Q_c we obtain the charge equations in the linear region as below

$$Q_g = W*L*C_{ox}(V_{gs} - V_{FB} - 2\phi_f - 0.5V_{ds} + \alpha_x V_{ds}^2/12(V_{gs} - V_t - 0.5\alpha_x V_{ds})) \quad (2.23a)$$

$$Q_b = W*L*C_{ox}(V_{FB} + 2\phi_f - V_t + 0.5(1 - \alpha_x)V_{ds} - (1 - \alpha_x)\alpha_x V_{ds}^2/12(V_{gs} - V_t - 0.5\alpha_x V_{ds})) \quad (2.23b)$$

$$Q_c = -W*L*C_{ox}(V_{gs} - V_t - 0.5\alpha_x V_{ds} + \alpha_x^2 V_{ds}^2/12(V_{gs} - V_t - 0.5\alpha_x V_{ds})) \quad (2.23c)$$

Saturation region: $V_t \leq V_{gs} < V_{gsat}$

The saturation region equations are obtained by integrating equation (2.20) from 0 to V_{dsat} and substituting the expression for ID in the saturation region in equation (2.21). Thus we get

$$\int_0^{V_{dsat}} Vy \frac{dy}{dVy}\, dVy = L^*(V_{gs} - V_t)/3\alpha_x$$

and

$$Q_g = W^*L^*C_{ox}(V_{gs} - V_{FB} - 2\phi_f - (V_{gs} - V_t)/3\alpha_x) \qquad (2.24a)$$

$$Q_b = W^*L^*C_{ox}(V_{FB} + 2\phi_f - V_t + (1 - \alpha_x)(V_{gs} - V_t)/3\alpha_x) \qquad (2.24b)$$

$$Q_c = -W^*L^*C_{ox}(2/3(V_{gs} - V_t)) \qquad (2.24c)$$

Subthreshold region: $V_{FB} + V_{bs} < V_{gs} < V_t$

$$Q_g = W^*L^*C_{ox}{}^*\frac{BE^2}{2}{}^*(-1 + (1 + 4(V_{gs} - V_{FB} - V_{bs})/BE^2)^{1/2}) \qquad (2.25a)$$

$$Q_b = -Q_g \qquad (2.25b)$$

$$Q_c = 0 \qquad (2.25c)$$

Accumulation region:

$$Q_g = W^*L^*C_{ox}(V_{gs} - V_t - V_{bs}) \qquad (2.26a)$$

$$Q_b = -Q_g \qquad (2.26b)$$

$$Q_c = 0 \qquad (2.26c)$$

The channel charge Q_c is partioned into Q_s and Q_d, i.e., source and drain charges by considering the following boundary conditions [6], [7].

(a) In the saturation region the channel is isolated from the drain; therefore, all the channel mobile charge Q_c goes into Q_s and Q_d is zero.

(b) Charges Q_d and Q_s are continous throughout the saturation and linear regions.

(c) The capacitances C_{dg} and C_{sg} are equal and the charges Q_d and Q_s are equal when V_{ds} is zero.

(d) The capacitances C_{dg}, C_{ds}, C_{db}, C_{sg}, C_{sd}, C_{sb} are continuous throughout the saturation and linear regions.

According to the above boundary conditions, Q_d and Q_s are given as follows.

Linear region:

$$Q_d = -W*L*C_{ox}(0.5(V_{gs} - V_t) - 0.75\alpha_x V_{ds} + \alpha_x^2 V_{ds}^2/8(V_{gs} - V_t - 0.5\alpha_x V_{ds})) \qquad (2.27a)$$

$$Q_s = -W*L*C_{ox}(0.5(V_{gs} - V_t) + 0.25\alpha_x V_{ds} - \alpha_x^2 V_{ds}^2/24(V_{gs} - V_t - 0.5\alpha_x V_{ds})) \qquad (2.27b)$$

Saturation region:

$$Q_d = 0$$

$$Q_s = -W*L*C_{ox}(2/3(V_{gs} - V_t)) \qquad (2.28)$$

Figure 2.3 shows the charges associated with the gate, bulk, source, and drain of a MOSFET device in all four regions using the above equations. The voltage dependent capacitances can be obtained by taking the partial derivatives of the charge equations with respect to different terminal voltages.

Let

$$C_{ij} = \frac{\partial Q_i}{\partial V_{ij}} \qquad (2.29)$$

where $i \neq j$ $i=g,b,d,s$

The above equation yields twelve capacitances to evaluate, three for each terminal of the device. Only nine of the twelve capacitances are independent. Therefore, if we choose to evaluate C_{gb}, C_{gd}, C_{gs}, C_{bg}, C_{bd}, C_{bs}, C_{dg}, C_{db}, C_{ds}, then the other three capacitances C_{sg}, C_{sb}, C_{sd} can be determined by

$$C_{sg} = C_{gb} + C_{gd} + C_{gs} - C_{bg} - C_{ds}$$

$$C_{sb} = C_{gb} + C_{bd} + C_{bs} - C_{gb} - C_{db}$$

$$C_{sd} = C_{dg} + C_{db} + C_{ds} - C_{gd} - C_{bd}$$

Figure 2.4 shows three of these twelve capacitances, i.e., C_{gd}, C_{gs}, and C_{gb} as a function of the gate to source voltage.

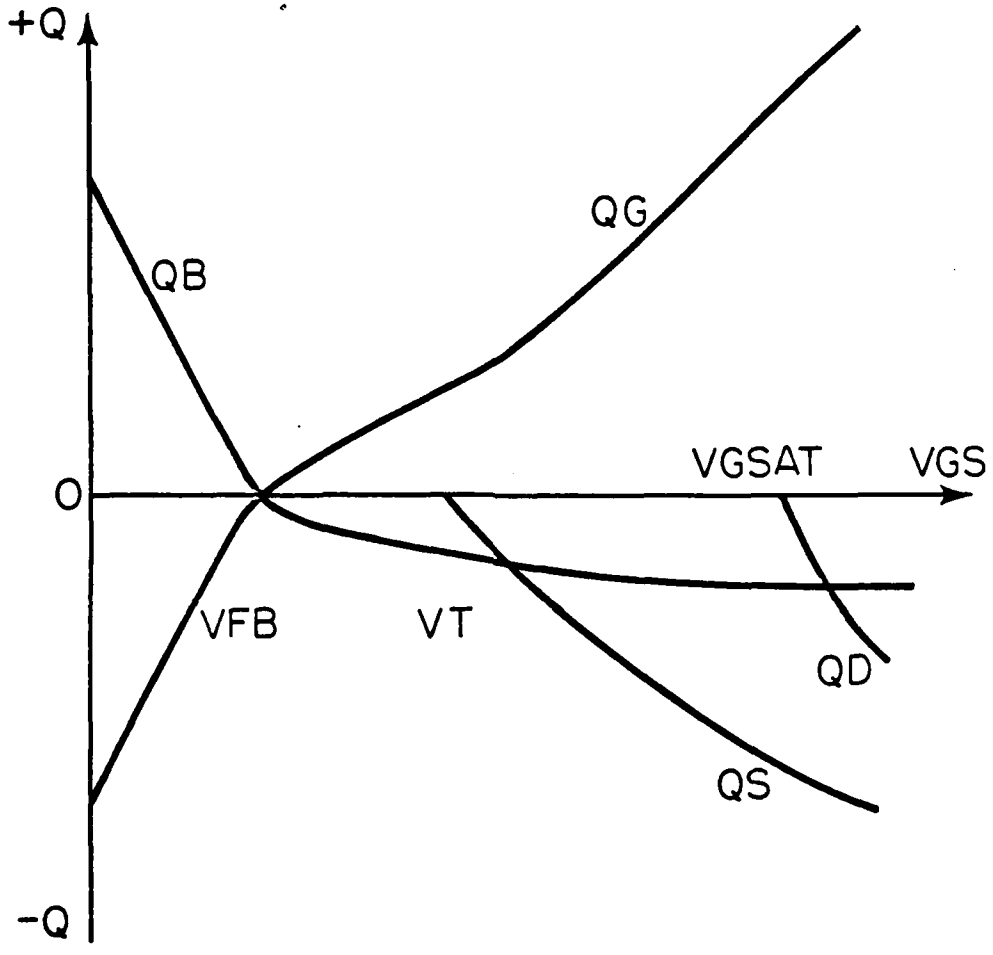


Figure 2.3 Voltage Dependent Charges

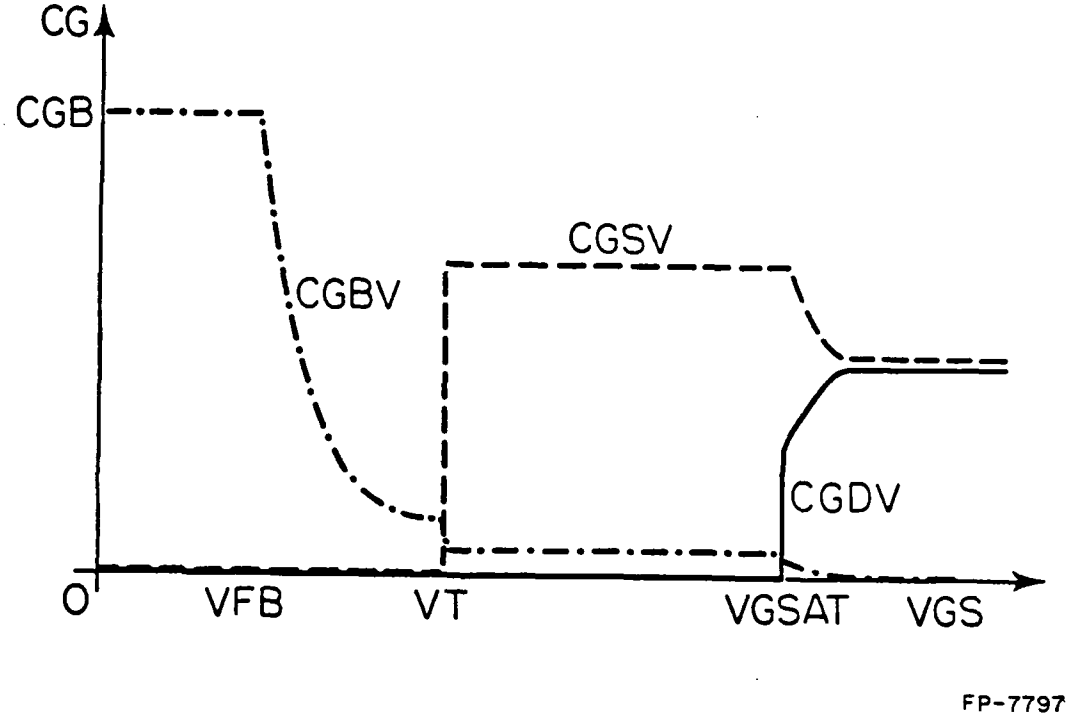


Figure 2.4 Voltage Dependent Gate Capacitances

2.2. Bipolar Transistor Model

The bipolar transistor model in SLATE is based upon the Gummel and Poon integral charge control model. The model reduces to the simpler Ebers-Moll model if the additional parameters are not specified.

Figure 2.5 shows the bipolar transistor model used in SLATE with the collector-substrate capacitance included. The DC equations for the transistor are as follows:

IBE = Area*IS*(EXP(VBE/VT) - 1) For VBE $\geq$ 0

IBE = Area*IS*VBE/VT For VBE < 0

IBC = Area*IS*(EXP(VBE/VT) -1) For VBC $\geq$ 0

IBC = Area*IS*VBC/VT For VBC < 0

IDE = Area*IS*C2*(EXP(VBE/VTE) - 1) For VBE $\geq$ 0

IDE = Area*IS*C2*VBE/VTE For VBE < 0

IDC = Area*IS*C4*(EXP(VBC/VTC) - 1) For VBC $\geq$ 0

IDC = Area*IS*C4*VBC/VTC For VBC < 0

IC = (IBE + IBC)/QB - IBC/BR - IDC

IB = IBE/BF + IDE + IDC + IBC/BR

where:

VT = K*T/Q

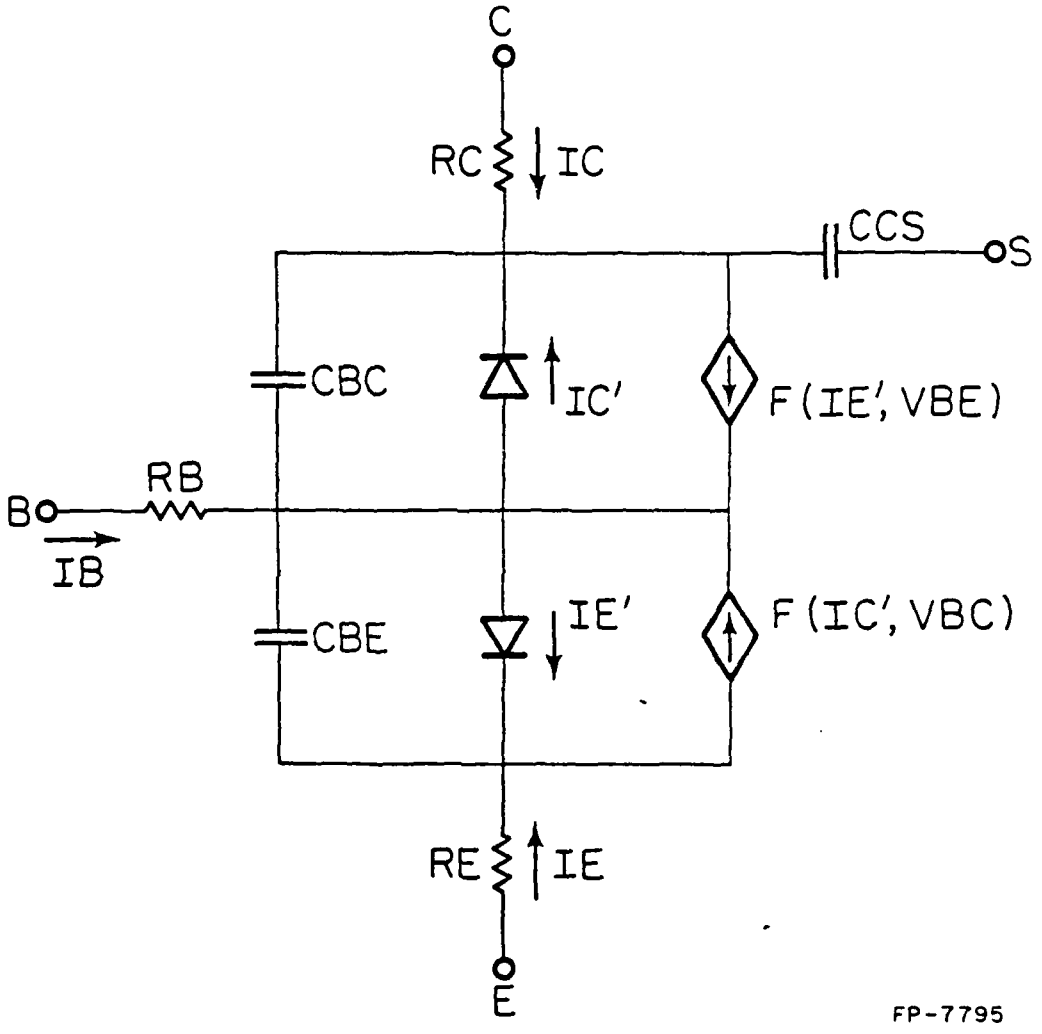


Figure 2.5 Bipolar Transistor Model

$$VTE = NE*K*T/Q$$

$$VTC = NC*K*T/Q$$

$$QB = Q1*(1 + (1 + 4*Q2)^{1/2})/2$$

$$Q1 = 1/(1- VBE/VB - VBC/VA)$$

$$Q2 = IBE/(Area*IK) + IBC/(Area*IKR)$$

In the above equations if the additional Gummel-Poon parameters, i.e., C2, IK, C4, IKR, and VB are not specified, then the model reduces to the Ebers-Moll model. The currents IDE and IDC are zero and QB=Q1.

The capacitor equations of the transistor are the sum of the *diffusion capacitances and the transition capacitances.*

$$CBE = Area*IS*(TF/VT)*EXP(VBE/VT) + Area*CJE*(1 + ME + VBE/PE)$$

For $VBE \geq 0$

$$CBE = Area*IS*(TF/VT)*VBE + Area*CJE/(1 - VBE/PE)^{ME}$$

For $VBE < 0$

$$CBC = Area*IS*(TR/VT)*EXP(VBC/VT) + Area*CJC*(1 + MC*VBC/PC)$$

For $VBC \geq 0$

$$CBC = Area*IS*(TR/VT)*VBC + Area*CJC/(1 - VBC/PC)^{MC}$$

For $VBC < 0$

CHAPTER 3

LATENCY EXAMPLES AND RESULTS

Digital circuits render themselves to the exploitation of the phenomenon of latency due to the inherent delay between excitation and response. This is specifically true for VLSI circuits in which a large percentage of the devices may be inactive in a given time interval. The parts of the circuit which are not active at any particular time are called latent. SLATE takes advantage of this latency phenomenon in real circuits and provides savings in execution time.

The savings in computer execution time are achieved mostly during the transient analysis by leaving the latent subnetworks out of the analysis, i.e., no linearization, no preprocessing of the subnetworks to eliminate internal variables, no backward substitution to solve for the internal subnetwork voltages, and no convergence tests are done on the parts of the network which are declared latent. SLATE does not automatically partition the network into subnetworks; therefore, the subcircuit command is used to specify the subnetworks. In other words the user must partition the circuit to be analysed into subcircuits, e.g., logic gates, etc., to take advantage of the latency scheme in SLATE.

3.1. Latency Criteria

In order to exploit the latency at the subnetwork level, some sort of criteria are required to determine if a subnetwork is latent. Ping Yang in his Ph.D. thesis [5] proposed four different schemes for the node tearing method. The scheme implemented in SLATE was shown to be

the most accurate and appropriate for the present version of SLATE. The scheme is as follows.

Consider a subnetwork N_k. Let the tearing node voltages of N_k be denoted by $\underline{V}_{tk}$, the charges of capacitors of subnetwork N_k be denoted by $\underline{Q}_k$, and the currents of capacitors of N_k be denoted by $\underline{I}_k$.

A subcircuit N_k is considered as latent if the following three conditions are satisfied.

(1) $$V_{tkm}(t_n) - V_{tkm}(t_{n-1}) \leq \varepsilon_a + \varepsilon_r \max(V_{tkm}(t_n) , V_{tkm}(t_{n-1})) \qquad m=1,2,\ldots,$$

where ε_a and ε_r are the absolute and relative error tolerances for voltages. This condition determines whether the changes in the tearing node voltages of the subnetwork N_k are small.

(2) $$I_{km}(t_n) - I_{km}(t_{n-1}) \leq \varepsilon_c + \varepsilon_r \max(I_{km}(t_n) , I_{km}(t_{n-1})) \qquad m=1,2,\ldots,$$

where ε_c is the absolute error tolerance for current. This condition is used to check if the changes of the energy storage elements of subnetwork N_k are small.

(3) $$h_{n-1} \frac{I_{km}(t_n) - I_{km}(t_{n-1})}{Q_{km}(t_n) - Q_{km}(t_{n-1})} \geq 1 \qquad m=1,2,\ldots,$$

where h_{n-1} is the time step taken by the program at t_{n-1}. This

condition is used to check if there are slowly varying nodes within the subnetwork N_k.

The subnetwork N_k will remain latent as long as

$$(4)\quad V_{tkm}(t_{n+j}) - V_{tkm}(t_{n-1}) \leq \varepsilon_a + \varepsilon_r \max(V_{tkm}(t_{n+j}) , V_{tkm}(t_{n-1})) \qquad m=1,2,\ldots,$$

The percentage Latency in the program SLATE is calculated by the following formula;

Latency = 1 - inlatn/itotal

Where inlatn = Number of nonlatent subcircuits times the number of iterations for those subcircuits.

itotal = Total number of subcircuits times the total number of iterations.

3.2. Experimental Results

A number of example circuits were simulated in an attempt to benchmark SLATE against SPICE2 (Version G.1)[1]. In this section, a small selection of examples is presented to give a comparison between the transient analysis portion of the two simulators.

In order to see the latency advantage in SLATE, the circuits chosen were an iterative array of a few basic subnetworks. The array size was varied to obtain a range of execution time. The idea was to show the following relationship between the execution time and the number of

[1] Version G.5A was not used due to convergence problems for some of the example circuits we simulated.

devices in the circuit.

$$t \propto x^n$$

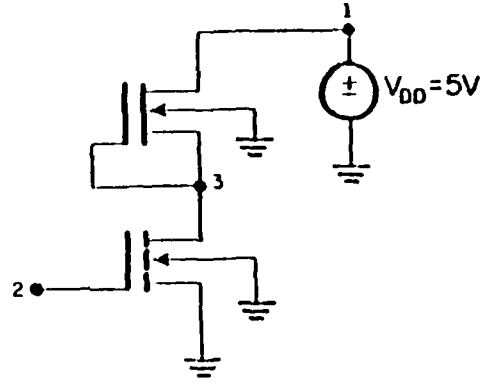
where t is the time taken for transient analysis, x is the number of transistors, and n is the rate at which the time increases with the increasing size of the circuit. The problem with the above approach is that, as the circuit size increases, the transient interval for which the circuit is simulated also increases. This does not give a true measure of the execution time t as a function of circuit size only. In order to resolve this problem, the execution time t was normalized to t' by dividing the execution time with the respective time interval, for which the circuit was simulated. Therefore, we hoped to show that

$$t' \propto x^n$$

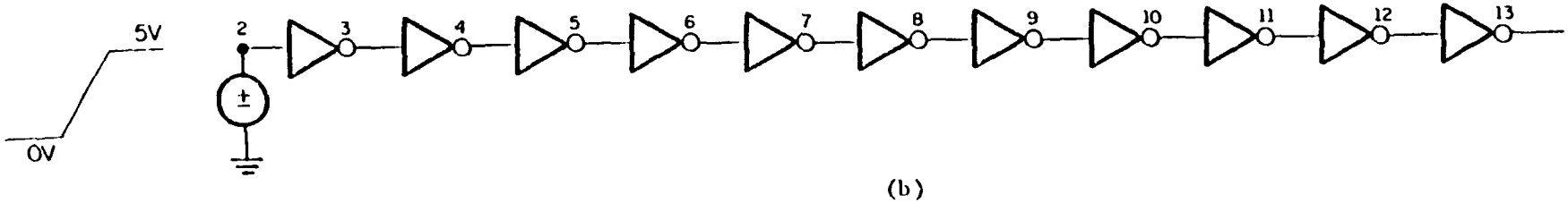
and that the rate of increase n, in SLATE is considerably less than that in SPICE2.

1.1.1. Example 3.1

Figure 3.1 shows the chain of inverters circuit which was analyzed by SLATE and SPICE2. This circuit has inherent latency which increases with the number of levels of logic gates. The number of levels was increased from 2 to 25, which resulted in an almost no latency to 46% latency at 25 levels in SLATE. Tables 3.1(a) and 3.1(b) summarize the results of these simulations. It may be noted that even at no latency SLATE takes less than half the time taken by SPICE2 (Version G.1). This is due to other features in SLATE, like a better reordering scheme, a



(a)



(b)

Figure 3.1(a) Subcircuit: An NMOS Inverter Gate
(b) A Chain of Inverters

Table 3.1(a) Chain of Inverters (SLATE)

INVERTERS	PERIOD	NUMTTP	NUMNIT	TRANAN	MOSFETS	LATENCY
2	36ns	61	137	7.55s	4	.0304
4	46ns	62	161	14.2s	8	.1214
6	56ns	62	172	22.4s	12	.1755
8	66ns	71	217	32.3s	16	.2632
10	76ns	63	197	36.2s	20	.3072
20	126ns	63	255	73.8s	40	.4600
25	176ns	64	258	96.1s	50	.4231

Table 3.1(b) Chain of Inverters (SPICE)

INVERTERS	PERIOD	NUMTTP	NUMNIT	TRANAN	MOSFETS
2	36ns	76	192	15.6s	4
4	46ns	77	211	29.0s	8
6	56ns	87	252	53.6s	12
8	66ns	90	264	73.0s	16
10	76ns	97	295	102.1s	20
20	126ns	129	456	264.2s	40
25	176ns	156	560	407.8s	50

where

PERIOD = Simulation interval (nanoseconds).

NUMTTP = Number of time points.

NUMNIT = Number of iterations for transient analysis.

TRANAN = Transient analysis time (seconds).

piecewise nonlinear approach which reduces the number of iterations needed to find the solution, and a more optimized code. Figure 3.2 shows a graph of normalized time against the number of transistors. Even though the initial slope of both the curves is about the same, i.e., n=0.59 for SLATE and n=0.72 for SPICE2, it gets higher n=1.03 for SPICE2 and lower n=0.33 for SLATE, as the number of devices increases ($x \geq 20$). This shows a rate of increase in SPICE2 three times higher than in SLATE. Therefore, in this particular example a clear advantage of the latency scheme is seen. The input deck used in this example is given in the Appendix (sec. A.10) at the end of the thesis.

3.2.2. Example 3.2

In this example a more complex circuit was analyzed. The number of levels of logic gates is small and the interconnection network is more complicated. The circuit is a full adder circuit realized by MOS NAND gates, as shown in Figure 3.3. Level 2 MOS model was used in SPICE2 and the charge conserving MOS model described in Chapter 2 was used in SLATE. The number of adder stages was increased from one, to two, to four, and the circuit was exercised with two different patterns of inputs. The first pattern applied was the one in which all the inputs to the adder were changed from 0 to 5V. This case, referred to as "all" from here on, resulted in maximum activity in the circuit. In the second pattern applied, only one input of the first stage was changed. This case, referred to as "one" from here on, resulted in minimum activity in the circuit. The above two cases were simulated on SLATE, with and without taking advantage of the latency scheme. Tables 3.2(a), 3.2(b),and 3.2(c) summarize the simulation results for the "all" case,

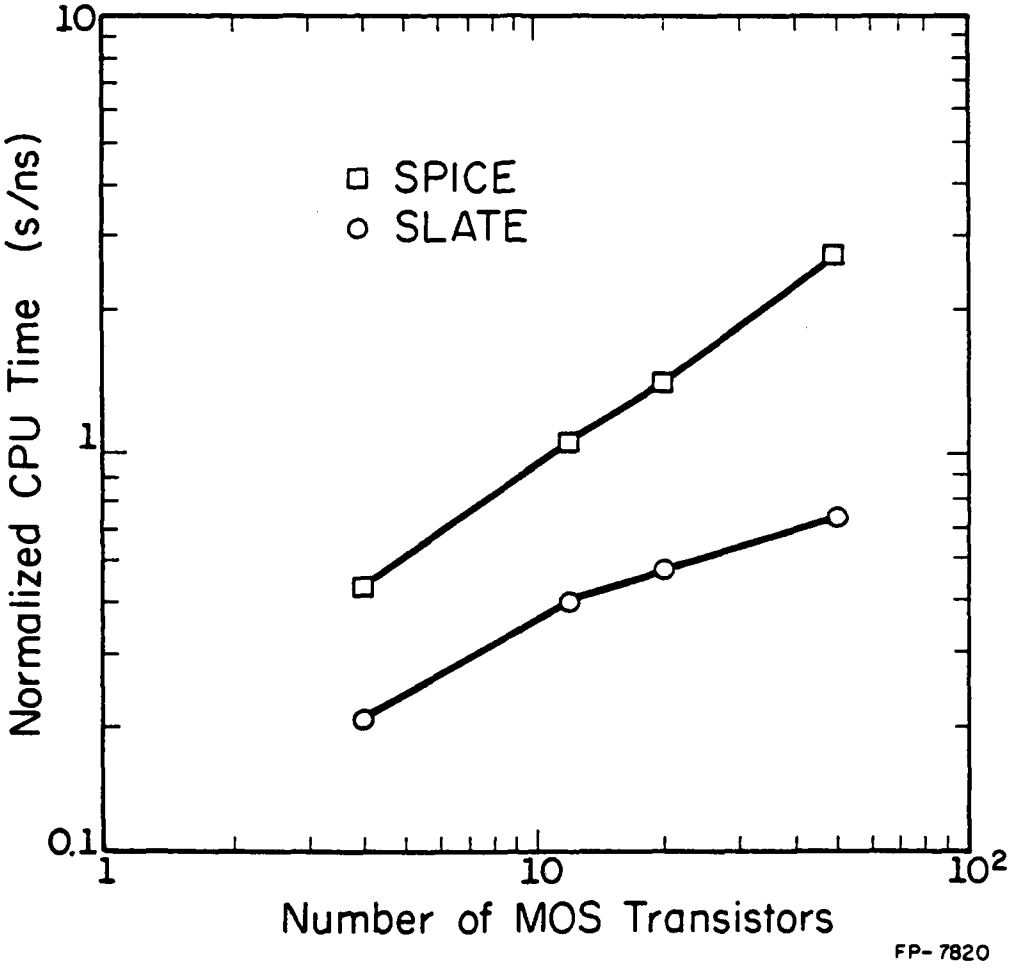


Figure 3.2 Simulation Data for Chain of Inverters

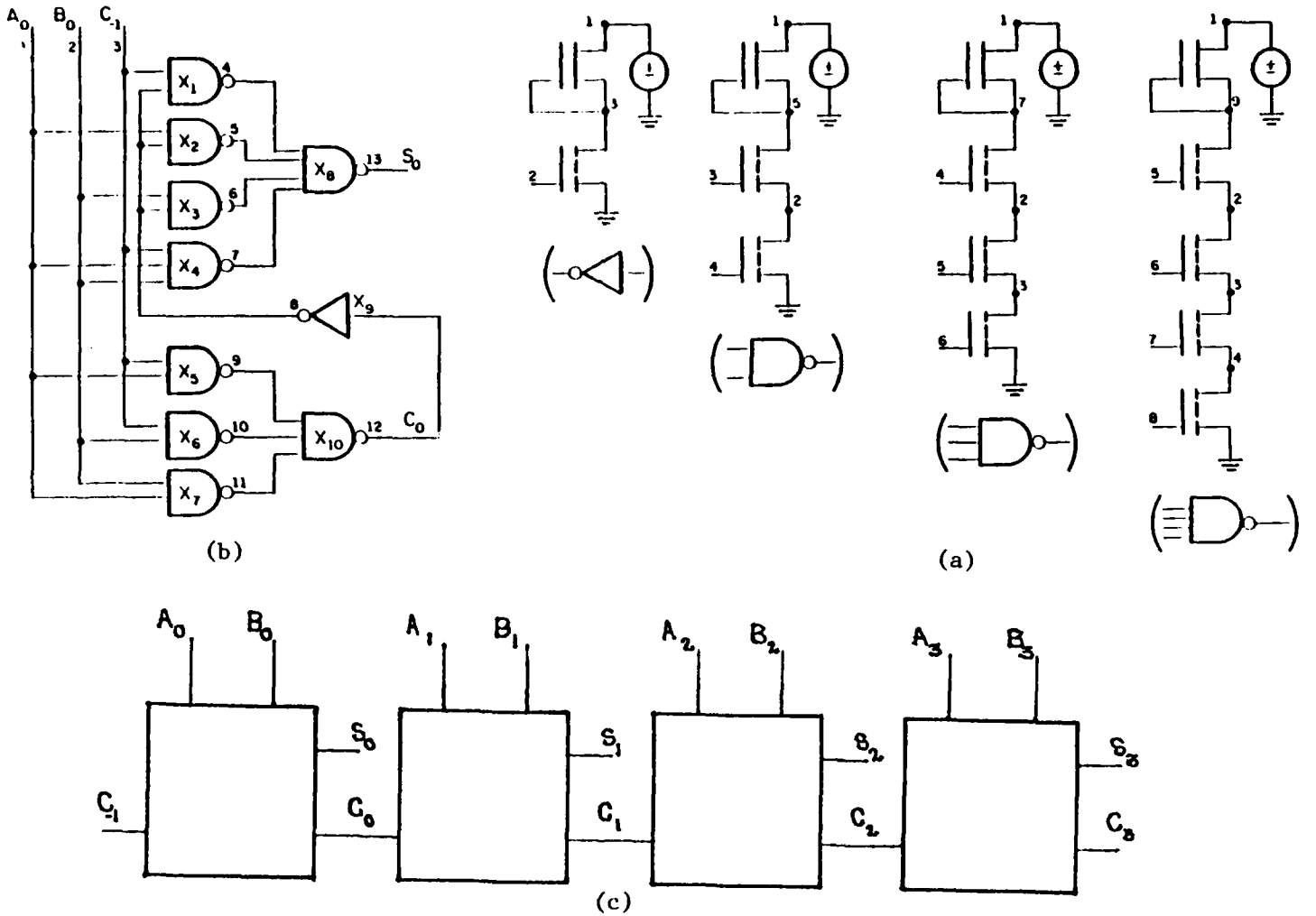


Figure 3.3(a) Subcircuits (b) One Bit Full Adder
(c) Four Bit Adder

and Tables 3.3(a), 3.3(b), and 3.3(c) summarize the results for the "one" case. These results were obtained for an absolute current error tolerance of 1 microamp, due to the convergence problems in SPICE2 for a tighter error tolerance of 1 picoamp.

Figure 3.4 shows the graph of these simulation results. Case "all" is denoted by solid squares for SPICE2, solid circles for SLATE with latency exploitation, and hollow triangles for SLATE without latency exploitation. Case "one" is denoted by hollow squares for SPICE2, hollow circles for SLATE with latency exploitation, and solid triangles for SLATE without latency exploitation. Several conclusions can be made from the curves, which are as follows.

In the case "all", SPICE2 shows an increase in slope from n=0.373 to n=0.658 as the number of adder stages increases from two to four, whereas, SLATE with latency exploitation shows a constant rate of increase n=0.483, which is less than the rate of increase in SPICE2 for two or more adder stages. SLATE without latency exploitation initially shows a rate of increase which is approximately the same as in SLATE with latency exploitation. It may also be noted that, in SLATE, the case without latency takes a lesser amount of transient analysis time than the case with latency exploitation for adder stages less than two, but the rate of increase, in the no latency exploitation case, increases from n=0.469 to n=0.693 as the stages increase. This may be explained by the fact that for less than two stages the circuit does not have very much latency, but an additional overhead is paid in expanding the subcircuits and checking the criteria in the latency exploitation case.

Table 3.2(a) Adder Circuit-- All Inputs Changing (SLATE with Latency)

STAGES	PERIOD	NUMTTP	NUMNIT	TRANAN	MOSFETS	LATENCY
1	125ns	58	159	61.1s	33	.1159
2	195ns	58	197	133.2s	66	.2199
4	265ns	58	202	252.9s	132	.2305

Table 3.2(b) Adder Circuit-- All Inputs Changing (SLATE without Latency)

STAGES	PERIOD	NUMTTP	NUMNIT	TRANAN	MOSFETS	LATENCY
1	125ns	58	159	55.1s	33	0
2	195ns	58	184	119.0s	66	0
4	265ns	58	199	261.4s	132	0

Table 3.2(c) Adder Circuit— All Inputs Changing (SPICE)

STAGES	PERIOD	NUMTTP	NUMNIT	TRANAN	MOSFETS
1	125ns	112	325	184.0s	33
2	195ns	102	311	371.7s	66
4	265ns	102	334	767.0s	132

Table 3.3(a) Adder Circuit— One Input Changing (SLATE with Latency)

STAGES	PERIOD	NUMTTP	NUMNIT	TRANAN	MOSFETS	LATENCY
1	125ns	58	142	43.9s	33	.2556
2	195ns	58	142	79.6s	66	.3327
4	265ns	58	148	146.4s	132	.4079

Table 3.3(b) Adder Circuit— One Input Changing (SLATE without Latency)

STAGES	PERIOD	NUMTTP	NUMNIT	TRANAN	MOSFETS	LATENCY
1	125ns	58	142	45.7s	33	0
2	195ns	58	138	85.5s	66	0
4	265ns	58	143	168.6s	132	0

Table 3.3(c) Adder Circuit— One Input Changing (SPICE)

STAGES	PERIOD	NUMTTP	NUMNIT	TRANAN	MOSFETS
1	125ns	80	171	107.0s	33
2	195ns	79	175	206.9s	66
4	265ns	73	156	365.2s	132

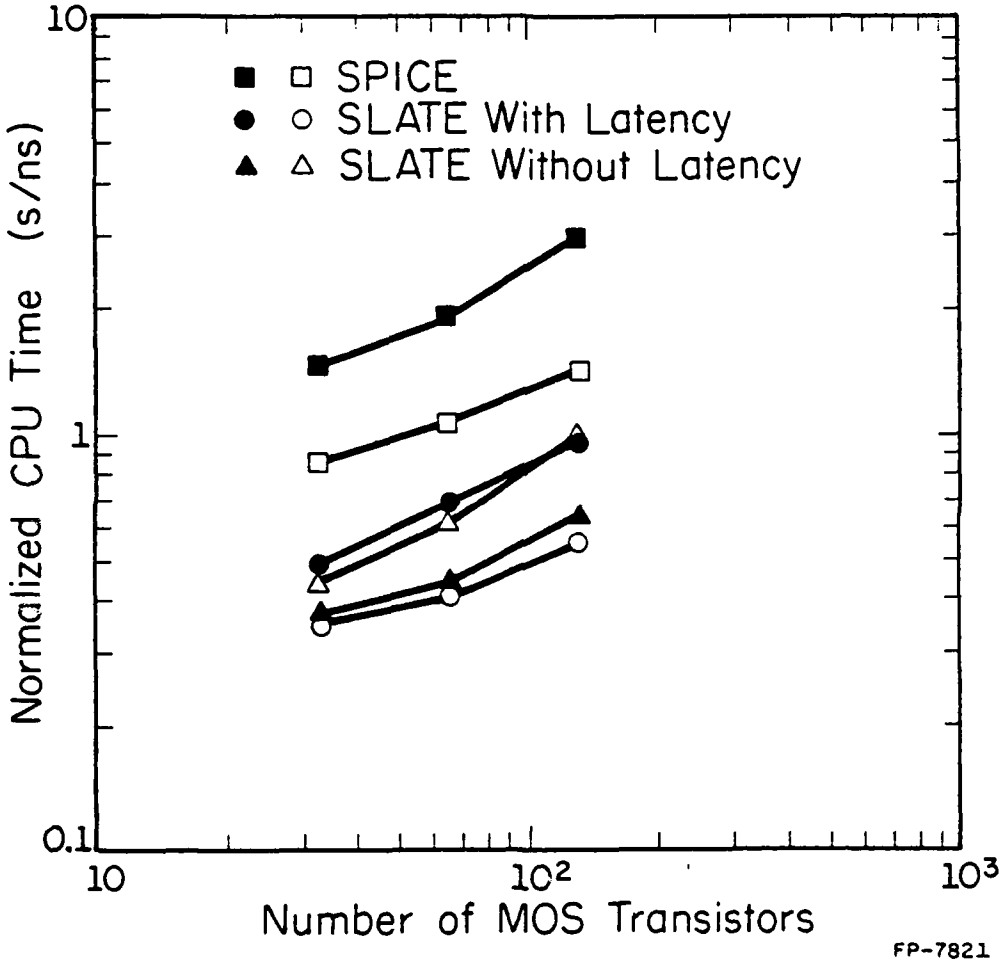


Figure 3.4 Simulation Data for Adder Circuit

In the "one" case, the transient analysis time taken in all three cases is reduced due to lesser activity in the circuit. This is because SPICE2 has latency exploitation at the device level, i.e., if the solution has not changed from the previous time point, the nonlinear devices are not linearized, and the previous time point results are used. Also, since there is less activity in the circuit, the step size taken by the program increases. These two facts account for the decrease in transient analysis time in SPICE2. In SLATE, it may be noted that the latency exploitation scheme starts paying off from the very beginning. This is due to the fact that the circuits have more latency (i.e., from Table 3.3(a) latency exploitation is from 25.5% to 40.8%). The input data deck for this example is included in the Appendix (sec. A.10) at the end of the thesis.

APPENDIX

USER'S GUIDE TO SLATE

SLATE (a Simulator with Latency and Tearing) is an electronic circuit simulation program that was originally developed from SPICE2 by Ping Yang of The Coordinated Science Laboratory and the Department of Electrical Engineering at The University of Illinois [5] and later modified by Ping Yang at the Central Research Laboratory of Texas Instruments. SLATE is particularly well suited for the simulation of Large Scale Integrated (LSI) circuits due to the implementation of algorithms which exploit the repetitiveness and latency properties in these circuits. Exploitation of these properties provides savings in the storage requirements and computation time, the two very important resources for LSI circuit simulators. Circuits simulated may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, and the four most common semiconductor devices: diodes, BJT's, JFET's, and MOSFET's. SLATE has built-in models for the semiconductor devices, and the user need specify only the pertinent model parameter values. The model for the BJT is based on the integral charge model of Gummel and Poon [8]; however, if the Gummel-Poon parameters are not specified, the model reduces to the simpler Ebers-Moll model. In either case, charge storage effects and ohmic resistances may be included. The diode model can be used for either junction diodes or Schottky barrier diodes. The JFET model is based on the FET model of Shichman and Hodges [17]. The MOSFET model is a modified Shichman and Hodges model developed by Ping Yang

[6], [7]. The model is charge conserving with short channel and subthreshold effects built into it.

A.1. Types of Analysis

A.1.1. DC analysis

The dc analysis portion of SLATE determines the dc operating point of the circuit with capacitors opened and inductors shorted. A dc analysis is automatically performed prior to a transient analysis to determine the transient initial conditions. The dc analysis can also be used to generate dc transfer curves: a specified independent voltage or current source is stepped over a user-specified range and the dc output variables are stored for each sequential source value. The dc analysis options are specified on the .DC and .OP control cards.

If one desires to see the small-signal models for nonlinear devices in conjunction with a transient analysis operating point, then the .OP card must be provided. The dc bias conditions will be identical for each case, but the more comprehensive operating point information is not available to be printed when transient initial conditions are computed.

A.1.2. Transient analysis

The transient analysis portion of SLATE computes the transient output variables as a function of time over a user specified time

interval. The initial conditions are automatically determined by a dc analysis. All sources which are not time dependent (for example, power supplies) are set to their dc value. The transient time interval is specified on the .TRAN card.

A.1.3. Analysis at different temperatures

All input data for SLATE are assumed to have been measured at 27 deg C (300 deg K). The simulation also assumes a nominal temperature of 27 deg C. The circuit can be simulated at other temperatures by using a .TEMP control line.

A.2. Convergence

Both dc and transient solutions are obtained by an iterative process which is terminated when both of the following conditions hold:

1) The nonlinear branch currents converge to within a tolerance of 0.1 percent or 1 picoamp (1.0E-12 Amp), whichever is larger.

2) The node voltages converge to within a tolerance of 0.1 percent or 1 microvolt (1.0E-6 Volt), whichever is larger.

Although the algorithm used in SLATE has been found to be very reliable, in some cases it will fail to converge to a solution. When this failure occurs, the program will print the node voltages at the last iteration and terminate the job. In such cases, the node voltages that are printed are not necessarily correct or even close to the correct solution.

Failure to converge in the dc analysis is usually due to an error in specifying circuit connections, element values, or model parameter values. Regenerative switching circuits or circuits with positive feedback probably will not converge in the dc analysis unless the OFF option is used for some of the devices in the feedback path, or the .FORCE card is used to force the circuit to converge to the desired state.

A.3. Input Format

The input format for SLATE is of the free format type. Fields on a card are separated by one or more blanks, a comma, an equal (=) sign, or a left or right parenthesis; extra spaces are ignored. A card may be continued by entering a + (plus) in column 1 of the following card; SLATE continues reading beginning with column 2.

A name field must begin with a letter (A through Z) and cannot contain any delimiters. Only the first eight characters of the name are used.

A number field may be an integer field (10, -20), a floating point field (3.14159), either an integer or floating point number followed by an integer exponent (3E-11, 1.25E4), or either an integer or a floating point number followed by one of the following scale factors:

t=1E12	g=1E9	meg=1E6	k=1E3	mil=25.4E-6
m=1E-3	u=1E-6	n=1E-9	p=1E-12	f=1E-15

Letters immediately following a number that are not scale factors are ignored, and letters immediately following a scale factor are ignored. Hence, 10, 10V, 10VOLTS, and 10HZ all represent the same number, and M, MA, MSEC, and MMHOS all represent the same scale factor. Note that 1000, 1000.0, 1E3, 1.0E3, and 1K all represent the same number.

A.4. Circuit Description

The circuit to be analyzed is described to SLATE by a set of element cards, which define the circuit topology and element values, and a set of control cards, which define the model parameters and the run controls. The first card in the input deck must be a title card, and the last card must be a .END card. The order of the remaining cards is arbitrary (except, of course, that continuation cards must immediately follow the card being continued).

Each element in the circuit is specified by an element card that contains the element name, the circuit nodes to which the element is connected, and the values of the parameters that determine the electrical characteristics of the element. The first letter of the element name specifies the element type. The format for the SLATE element types is given in what follows. The strings XXXXXXX, YYYYYYY, and ZZZZZZZ denote arbitrary alphanumeric strings. For example, a resistor name must begin with the letter R and can contain from one to eight characters. Hence, R, R1, RSE, ROUT, and R3AC2ZY are valid resistor names. Data fields that are enclosed in lt '<' and gt '>'

signs are optional. All indicated punctuation (parentheses, equal signs, etc.) are required. With respect to branch voltages and currents, SLATE uniformly uses the associated reference convention (current flows in the direction of voltage drop).

Nodes must be nonnegative integers but need not be numbered sequentially. The datum (ground) node must be numbered zero. Each node in the circuit must have a dc path to ground. Every node must have at least two connections except for MOSFET substrate nodes (which have two internal connections anyway).

A.5. Title Card; Comment Cards; and End Card

A.5.1. Title card

Examples:

```
DYNAMIC BOOTSTRAP CIRCUIT
```

This card must be the first card in the input deck. Its contents are printed as the heading for each section of output.

A.5.2. End card

Examples:

```
.END
```

This card must always be the last card in the input deck. Note

that the period is an integral part of the name.

A.5.3. Comment card

General Form

* <any comment>

Examples:

* STAGE ONE OF RIPPLE CARRY ADDER

* MAY THE FORCE BE WITH MY CIRCUIT

The asterisk in the first column indicates that this card is a comment card. Comment cards may be placed anywhere in the circuit description.

A.6. Element Cards

A.6.1. Resistors

General form

RXXXXXXX N1 N2 VALUE

Examples:

R1 1 2 100

RC1 12 17 1K

N1 and N2 are the two element nodes. VALUE is the resistances (in ohms) and may be positive or negative but not zero.

A.6.2. Capacitors and inductors

General form

CXXXXXXX N+ N- VALUE <IC=INCOND>

LYYYYYYY N+ N- VALUE <IC=INCOND>

Examples:

CBYP 13 0 1UF

COSC 17 23 10U IC=3V

LLINK 10 12 1UH

LSHUNT 2 3 5U IC=10.5MA

N+ and N- are the positive and negative element nodes, respectively. VALUE is the capacitance in Farads or inductance in Henries. The (optional) initial condition is the initial (time-zero) value of capacitor voltage (in volts) or initial (time-zero) value of inductor current (in amperes) that flows from N+, through the inductor, to N-. Note that the initial conditions (if any) apply 'only' if the UIC option is specified on the .TRAN card.

Nonlinear capacitors and inductors can be described as ;

General form

CXXXXXXX N+ N- POLY C0 C1 C2 ... <IC=INCOND>

LYYYYYYY N+ N- POLY L0 L1 L2 ... <IC=INCOND>

C0 C1 C2 ... (and L0 L1 L2 ...) are the coefficients of a polynomial describing the element value. The capacitance is expressed as a function of the voltage across the element, while the inductance is a

function of the current through the inductor. The value is computed as

value=C0+C1*V+C2*V**2+...

value=L0+L1*I+L2*V**2+...

where V is the voltage across the capacitor and I is current through the inductor.

A.6.3. Coupled mutual inductors

General form

KXXXXXXX LYYYYYYY LZZZZZZZ VALUE

Examples:

K10 LAA LBB 0.99

KL1L2 L1 L2 0.8

LYYYYYYY and LZZZZZZZ are the names of the two coupled inductors, and VALUE is the coefficient of coupling, K, which must be greater than 0 and less than or equal to 1. Using the 'dot' convention, place a 'dot' on the first node of each inductor.

A.6.4. Linear dependent sources

SLATE allows circuits to contain linear dependent sources characterized by any of the four equations

i=g*v v=e*v i=f*i v=h*i

where g, e, f, and h are constants representing transconductance,

voltage gain, current gain, and transresistance, respectively.

A.6.4.1. Linear voltage controlled current sources

General form

GXXXXXXX N+ N- NC+ NC- VALUE

Examples:

G1 2 0 5 0 0.1MMHO

N+ and N- are the positive and negative nodes, respectively. Current flow is from the positive node, through the source, to the negative node. NC+ and NC- are the positive and negative controlling nodes, respectively. VALUE is the transconductance (in mhos).

A.6.4.2. Linear voltage controlled voltage sources

General form

EXXXXXXX N+ N- NC+ NC- VALUE

Examples:

E1 2 3 14 1 2.0

N+ is the positive node, and N- is the negative node. NC+ and NC- are the positive and negative controlling nodes, respectively. VALUE is the voltage gain.

A.6.4.3. Linear current controlled current sources

General form

FXXXXXXX N+ N- VNAM VALUE

Examples:

F1 13 5 VSENS 5

N+ and N- are the positive and negative nodes, respectively. Current flow is from the positive node, through the source, to the negative node. VNAM is the name of a voltage source through which the controlling current flows. The direction of positive controlling current flow is from the positive node, through the source, to the negative node of VNAM. VALUE is the current gain.

A.6.4.4. Linear current controlled voltage sources

General form

HXXXXXXX N+ N- VNAM VALUE

Examples:

HX 5 17 VZ 0.5K

N+ and N- are the positive and negative nodes, respectively. VNAM is the name of a voltage source through which the controlling current flows. The direction of positive controlling current flow is from the positive node, through the source, to the negative node of VNAM. VALUE

is the transresistance (in ohms).

A.6.5. Independent sources

General form

VXXXXXXX N+ N- <<DC> DC/TRAN VALUE>

IYYYYYYY N+ N- <<DC> DC/TRAN VALUE>

Examples:

VCC 10 0 DC 6

VMEAS 12 9

N+ and N- are the positive and negative nodes, respectively. Note that voltage sources need not be grounded. Positive current is assumed to flow from the positive node, through the source, to the negative node. A current source of positive value will force current to flow from the N+ node, through the source, and into the N- node. Voltage sources, in addition to being used for circuit excitation, are the 'ammeters' for SLATE, that is, zero valued voltage sources may be inserted into the circuit for the purpose of measuring current. They will, of course, have no effect on circuit operation since they represent short circuits.

DC/TRAN is the dc and transient analysis value of the source. If the source value is zero both for dc and transient analyses, this value may be omitted. If the source value is time-invariant (e.g., a power supply), then the value may optionally be preceded by the letters DC.

Any independent source can be assigned a time-dependent value for transient analysis. If a source is assigned a time-dependent value, the time-zero value is used for dc analysis. There are four independent source functions: pulse, exponential, piece-wise linear, and sinusoidal. If parameters other than source values are omitted or set to zero, the default values shown will be assumed. (TSTEP is the printing increment and TSTOP is the final time (see the .TRAN card for explanation)).

Pulse: PULSE(V1 V2 TD TR TF PW PER)

Examples:

VIN 3 0 PULSE(-5 5 1NS 1NS 1NS 50NS 100NS)

parameters	default values	units
V1 (initial value)		volts or amps
V2 (pulsed value)		volts or amps
TD (delay time)	0.0	seconds
TR (rise time)	0.0	seconds
TF (fall time)	0.0	seconds
PW (pulse width)	TSTOP	seconds
PER(period)	TSTOP	seconds

A single pulse so specified is described by the following table:

time	value
0	V1
TD	V1
TD+TR	V2
TD+TR+PW	V2
TD+TR+PW+TF	V1
TSTOP	V1

Intermediate points are determined by linear interpolation.

Exponential: EXP(V1 V2 TD1 TAU1 TD2 TAU2)

Examples:

VIN 3 0 EXP(-5 0 2NS 30NS 60NS 40NS)

parameters		default values	units
V1	(initial value)		volts or amps
V2	(pulsed value)		volts or amps
TD1	(rise delay time)	0.0	seconds
TAU1	(rise time constant)	TSTEP	seconds
TD2	(fall delay time)	TD1+TSTEP	seconds
TAU2	(fall time constant)	TSTEP	seconds

The shape of the waveform is described by the following table:

time	value
0 to TD1	V1
TD1 to TD2	V1+(V2-V1)*(1-exp(-(time-TD1)/TAU1))
TD2 to TSTOP	V1+(V2-V1)*(1-exp(-(time-TD1)/TAU1)) +(V1-V2)*(1-exp(-(time-TD2)/TAU2))

Piece-Wise Linear: PWL(T1 V1 <T2 V2 T3 V3 T4 V4 ...>)

Examples:

VCLOCK 7 5 PWL(0 -7 10NS -7 11NS -3 17NS -3 18NS -7 50NS -7)

Parameters and default values

Each pair of values (Ti, Vi) specifies that the value of the source is Vi in volts or amps) at time=Ti. The value of the source at intermediate values of time is determined by using linear interpolation on the input values

Sinusoidal: SIN(VO VA FREQ TD THETA)

Examples:

```
VIN 3 0 SIN(0 5 100MEG 1NS 1E10)
```

parameters		default value	units
VO	(offset)		volts or amps
VA	(amplitude)		volts or amps
FREQ	(frequency)	1/TSTOP	Hz
TD	(delay)	0.0	seconds
THETA	(damping factor)	0.0	1/seconds

The shape of the waveform is described by the following table:

time	value
0 to TD	VO
TD to TSTOP	VO + VA*exp(-(time-TD)*THETA)* sine(twopi*FREQ*(time+TD))

A.7. Semiconductor Devices

The elements that have been described to this point typically require only a few parameter values to specify completely the electrical characteristics of the element. However, the models for the four semiconductor devices that are included in the SLATE program require many parameter values. Moreover, many devices in a circuit often are defined by the same set of device model parameters. For these reasons, a set of device model parameters is defined on a separate .MODEL card and assigned a unique model name. The device element cards in SLATE then reference the model name. This scheme alleviates the need to specify all of the model parameters on each device element card.

Each device element card contains the device name, the nodes to which the device is connected, and the device model name. In addition,

other optional parameters may be specified for each device: geometric factors and an initial condition.

The area factor used on the diode, BJT and JFET device card determines the number of equivalent parallel devices of a specified model. The affected parameters are marked with an asterisk under the heading 'area' in the model descriptions below. Several geometric factors associated with the channel and the drain and source diffusions can be specified on the MOSFET device card.

Two different forms of initial conditions may be specified for devices. The first form is included to improve the dc convergence for circuits that contain more than one stable state. If a device is specified OFF, the dc operating point is determined with the terminal voltages for that device set to zero. After convergence is obtained, the terminal voltages are no longer held at zero and the program continues to iterate to obtain the exact value for the terminal voltages. If a circuit has more than one dc stable state, the OFF option can be used to force the solution to correspond to a desired state. If a device is specified OFF when in reality the device is conducting, the program will still obtain the correct solution (assuming the solutions converge) but more iterations may be required. The .INITIAL card serves a similar purpose as the OFF option. The .INITIAL option is easier to apply and is the preferred means to aid convergence.

The second form of initial conditions is specified for use with the transient analysis. These are true 'initial conditions' as opposed to the convergence aids above. See the description of .TRAN card for a

detailed explanation of initial conditions.

A.7.1. Device element cards

A.7.1.1. Junction diodes

General form

DXXXXXXX N+ N- MNAME <AREA> <OFF> <IC=VD>

Examples:

```
DOUT   7 8 DIODE1
DIN    3 7 DMOD 2.0 IC=0.3
```

N+ and N- are the positive and negative nodes, respectively. MNAME is the model name, AREA is the area factor, and OFF indicates an (optional) starting condition on the device for dc analysis. If the area factor is omitted, a value of 1.0 is assumed. The (optional) initial condition specification using IC=VD is intended for use with the UIC option on the .TRAN card, when a transient analysis is desired starting from other than the quiescent operating point.

A.7.1.2. Bipolar junction transistors (BJTs)

General form

QXXXXXXX NC NB NE <NS> MNAME <AREA> <OFF> <IC=VBE,VCE>

Examples:

```
Q5    10 20 30 QMOD IC=0.8,0.5
Q10   15 25 35 20 MOD1
```

NC, NB, and NE are the collector, base, and emitter nodes, respectively. NS is the (optional) substrate node. If unspecified, ground is used. MNAME is the model name, AREA is the area factor, and OFF indicates an (optional) initial condition on the device for the dc analysis. If the area factor is omitted, a value of 1.0 is assumed. The (optional) initial condition specification using IC=VBE,VCE is intended for use with the UIC option on the .TRAN card, when a transient analysis is desired starting from other than the quiescent operating point.

A.7.1.3. Junction field effect transistors (JFETs)

General form

JXXXXXXX ND NG NS MNAME <AREA> <OFF> <IC=VDS,VGS>

Examples:

J1 1 2 3 JMOD1 OFF

ND, NG, and NS are the drain, gate, and source nodes, respectively. MNAME is the model name, AREA is the area factor and OFF indicates an (optional) initial condition on the device for dc analysis. If the area factor is omitted, a value of 1.0 is assumed. The (optional) initial condition specification, using IC=VDS,VGS is intended for use with the UIC option on the .TRAN card, when a transient analysis is desired starting from other than the quiescent operating point.

A.7.1.4. MOSFETs

General form

MXXXXXXX ND NG NS NB MNAME <L=VAL> <W=VAL> <AD=VAL> <AS=VAL>
+ <ASD=VAL> <ASS=VAL> <RDD=VAL>
+ <RSS=VAL> <CGS=VAL> <CGD=VAL>
+ <CGB=VAL> <OFF> <IC=VDS,VGS,VBS>

Examples:

```
MIN 24 2  0  20 TYPE1
MLD 2  17 6  10 MODM L=5 W=2
MPT 2  16 6  10 MODM   5   2
M10 2  9  3  0  MOD1 L=10  W=5  AD=100  AS=100  ASD=40  ASS=40
M1  2  9  3  0  MOD1   10    5     2       2
```

ND, NG, NS, and NB are the *drain, gate, source,* and bulk (substrate) nodes, respectively. MNAME is the model name. L and W are the channel length and width, in microns or mils. AD and AS are the areas of the drain and source diffusion windows, while ASD and ASS are the areas of the drain and source sidewalls. The areas can be specified in micron^2 or mil^2. Figure A.1 shows the geometrical dimensions of a MOSFET device.The keyword MICRON or MIL can be used to specify micron or mil, respectively, on the .MODEL card. The default unit is micron. RDD and RSS represent the equivalent drain and source resistances. These resistances can be computed internally by SLATE, using the formula RXX = RX*AX/(W-WR)^2, where RX stands for RS and RD which are sheet resistances specified on the .MODEL card or the user may specify RSS and RDD on the MOSFET element card if the above does not correctly model the resistances. OFF indicates an (optional) initial condition on the

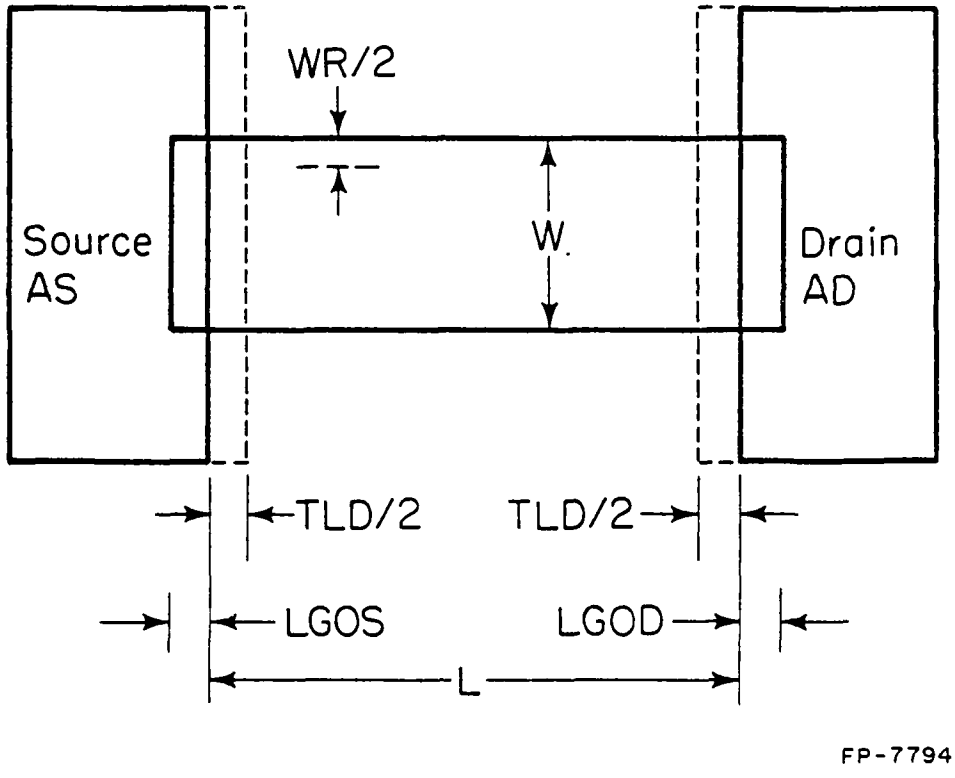


Figure A.1 MOSFET Geometrical dimensions

device for dc analysis. The (optional) initial condition specification using IC=VDS,VGS,VBS is intended for use with the UIC option on the .TRAN card, when a transient analysis is desired starting from other than the quiescent operating point.

A.7.2. MODEL card

General form

```
.MODEL MNAME TYPE(PNAME1=PVAL1 PNAME2=PVAL2 ... )
```

Examples:

```
.MODEL LOAD1 NMOS VTO=-2 KP=1E-5 BE=.52 COX=1F
```

The .MODEL card specifies a set of model parameters that will be used by one or more devices. MNAME is the model name, and TYPE is one of the following seven types:

NPN	NPN BJT model
PNP	PNP BJT model
D	diode model
NJF	N-channel JFET model
PJF	P-channel JFET model
NMOS	N-channel MOSFET model
PMOS	P-channel MOSFET model

Parameter values are defined by appending the parameter name, as given below for each model type, followed by an equal sign and the parameter value. Model parameters that are not given a value are assigned the default values given below for each model type.

A.7.2.1. Diode model

The dc characteristics of the diode are determined by the parameters IS and N. An ohmic resistance, RS, is included. Charge storage effects are modeled by a transit time, TT, and a nonlinear depletion layer capacitance which is determined by the parameters CJO, PHI, and M. The temperature dependence of the saturation current is defined by the parameters EG, the energy-gap and PT, the saturation current temperature exponent. The equation is as follows;

$$IS(T) = IS(TNOM)*EXP(EG*(T/TNOM-1)*Q/(N*K*T))*(T/TNOM)**(PT/N)$$

Table A.1 list the model parameters for the diode.

Table A.1 Diode Model Parameters

name	parameter	units	default	example	area
IS	saturation current	A	1.0E-14	1.0E-14	*
RS	ohmic resistance	Ohm	0	10	*
N	emission coefficient	-	1	1.0	
TT	transit-time	sec	0	0.1ns	
CJO	zero-bias junction capacitance	F	0	2pF	*
PHI	junction potential	V	1	0.6	
M	grading coefficient	-	0.5	0.5	
EG	activation energy	eV	1.11	1.11 Si 0.69 Sbd 0.67 Ge	
PT	saturation-current temperature exponent	-	3.0	3.0 jn 2.0 Sbd	

A.7.2.2. BJT model

The bipolar junction transistor model in SLATE is an adaptation of the integral charge control model of Gummel and Poon [8]. This modified Gummel-Poon model extends the original model to include several effects at high bias levels. The model will automatically simplify to the simpler Ebers-Moll model when certain parameters are not specified. The parameter names used in the modified Gummel-Poon model have been chosen to be more easily understood by the program user and to reflect better both physical and circuit design thinking.

The dc model is defined by the parameters IS, BF, NE, C2, and IK which determine the forward current gain characteristics, IS, BR, NC, C4, IKR, which determine the reverse current gain characteristics, and VA and VB which determine the output conductance for forward and reverse regions. Three ohmic resistances RB, RC, and RE are included. Base charge storage is modeled by forward and reverse transit times, TF and TR, and nonlinear depletion layer capacitances which are determined by CJE, PE, and ME for the B-E junction, CJC, PC, and MC for the B-C junction and CCS, for the C-S (Collector-Substrate) junction. The temperature dependence of the saturation current, IS, is determined by the energy-gap, EG, and the saturation current temperature exponent, PT. The model parameters for the BJT are listed in Table A.2. The temperature dependences are defined by the following equations;

$$IS(T) = IS(TNOM)*EXP(EG*(T/TNOM-1)*Q/(K*T))*(T/TNOM)**PT$$

$$C2(T) = C2(TNOM)*(IS(TNOM)/IS(T))**(1-1/NE)$$

$$C4(T) = C4(TNOM)*(IS(TNOM)/IS(T))**(1-1/NC)$$

Table A.2 BJT Model Parameters

name	parameter	units	default	example	area
BF	ideal forward beta	-	100	100	
BR	ideal reverse beta	-	1	0.1	
IS	saturation current	A	1.0E-14	1.0E-15	*
RB	base resistance	Ohms	0	100	*
RE	emitter resistance	Ohms	0	1	*
RC	collector resistance	Ohms	0	10	*
VA	forward Early voltage	V	infinite	200	
VB	reverse Early voltage	V	infinite	200	
IK	forward high-current knee current	A	infinite	10ma	*
C2	forward low-current nonideal base current coefficient	-	0	100	
NE	B-E emission coefficient	-	2	2	
IKR	reverse high-current knee current	A	infinite	10ma	*
C4	reverse low-current nonideal base current coefficient	-	0	1	
NC	B-C emission coefficient	-	2	2	
TF	forward transit time	sec	0	0.1ns	
TR	reverse transit time	sec	0	10ns	
CCS	zero-bias collector-substrate capacitance	F	0	2pF	*
CJE	B-E zero-bias depletion capacitance	F	0	2pF	*
PE	B-E built-in potential	V	1.0	0.7	
ME	B-E grading coefficient	-	0.5	0.5	
CJC	B-C zero-bias depletion capacitance	F	0	2pF	*
PC	B-C built-in potential	V	1.0	0.5	
MC	B-C grading coefficient	-	0.5	0.33	
EG	energy gap	eV	1.11	1.11 Si 0.67 Ge	
PT	saturation current exponent	-	3.0	3.0	

A.7.2.3. JFET model

The JFET model is derived from the FET model of Shichman and Hodges [17]. Table A.3 list the model parameters for the JFET. The dc characteristics are defined by the parameters VTO and BETA, which determine the variation of drain current with gate voltage, LAMBDA, which determines the output conductance, and IS,the saturation current of the two gate junctions. Two ohmic resistances, RD and RS, are included. Charge storage is modeled by nonlinear depletion layer capacitances for both gate junctions which vary as the -1/2 power of junction voltage and are defined by the parameters CGS, CGD, and PB. The temperature dependence of the saturation current,IS, is defined by the following equation;

$$IS(T) = IS(TNOM)*EXP(1.11*(T/TNOM-1)*Q/(K*T))$$

Table A.3 JFET Model Parameters

name	parameter	units	default	example	area
VTO	threshold voltage	V	-2.0	-2.0	
BETA	transconductance parameter	A/V^2	1.0E-4	1.0E-3	*
LAMBDA	channel length modulation parameter	1/V	0	1.0E-4	
RD	drain ohmic resistance	Ohm	0	100	*
RS	source ohmic resistance	Ohm	0	100	*
CGS	zero-bias G-S junction capacitance	F	0	5pF	*
CGD	zero-bias G-D junction capacitance	F	0	1pF	*
PB	gate junction potential	V	1	0.6	
IS	gate saturation current	A	1.0E-14	1.0E-14	*

A.7.2.4. MOSFET model

The dc characteristics of the MOSFET are defined by the device parameters VTO, KP, LAMBDA, THETA, PHI and BE. VTO is positive for enhancement mode and negative for depletion mode N-channel and P-channel devices. The short channel effects are modeled by the ALPHA, DE, and GAMMA parameters, and the subthreshold current is defined by parameters KPS and NG. Charge storage is modeled by three constant capacitors, CGS, CGD, and CFR, which represent overlap and fringing capacitances, by the nonlinear thin-oxide capacitance which is distributed among the gate, source, drain, and bulk regions, and by the nonlinear depletion-layer capacitances for both substrate junctions, divided into bottom and periphery, which vary as the M and MS power of junction voltage respectively, and are determined by the parameters CBD, CBS, KPN, M, MS and PB. Table A.4 list the model parameters for the MOSFET. The temperature dependence of the parameters N, IS, KP, KPS, and VTO are defined as follows;

$$N(T) = 5.884E+15*EXP(-0.555*Q/K*T)*T**1.5$$

$$IS(T) = IC(TNOM)*(T/TNOM)**3*EXP(1.11*(T/TNOM-1)*Q/K*T)$$

$$KP(T) = KP(TNOM)*(T/TNOM)**TCKP$$

$$KPS(T) = KPS(TNOM)*(T/TNOM)**(1.5+TCKP)$$

$$VTO(T) = VTO(TNOM)+TCVT*(T-TNOM)$$

Table A.4 MOSFET Model Parameters

name	parameter	units	default	example
VTO	zero-bias threshold voltage	V	0.0	1.0
N	bulk doping concentration	cm^{-3}	1e15	1e15
KP	constant($\mu_n * \varepsilon_{si}/(2*T_{ox})$)	A/V^2	0.0	1.0E-5
BE	body effect parameter $BE = (2\varepsilon_{si} qNa)^{1/2}/C_{ox}$	$V^{.5}$	0.0	0.52
LAMBDA	channel length modulation	-	0.01	0.05
RD	drain sheet resistance	Ohm/Sq	0.0	35.0
RS	source sheet resistance	Ohm/Sq	0.0	35.0
COX	thin oxide capacitance	F/mil^2 $micron^2$	1.0fF	$0.5fF/\mu m^2$
TLD	sum total of lateral diffusion of source and drain	mils or microns	0.0	1.0
LGO	length of gate overlap	mils or microns	0.0	0.0
KPN	constant which models diffusion capacitance $KPN = (q\varepsilon_{si} Na/2)^{1/2}$	$V^{.5}$ F	1.0fF	.1fF
THETA	mobility variation factor	1/V	0.028	0.028
IS	bulk junction saturation current	A/mil^2 $A/micron^2$	1.0E-14	1.0E-15
TCVT	temperature coefficient of VTO	V/deg C	-3E-3	-6E-3
TCKP	temperature coefficient of KP	-	-1.5	-1.4
ALPHA	KPlinear/KPsaturation	-	1.0	1.2
NS	channel stop impurity concentration	cm^{-3}	1E16	1E16
NG	subthreshold parameter	-	1.0	0.9
FC	forward bias nonideal junction capacitance coefficient	-	0.5	0.5
WR	width reduction factor for channel stop out-diffusion	mils or microns	0.0	0.0

Table A.4 (cont.)

LR	mask tolerance length reduction	mils or microns	0.0	0.0
M	PN junction grading coefficient	-	0.5	0.5
KPS	subthreshold parameter	-	0.0	0.0
LGOD	length of gate-drain overlap	mils or microns	LGO	0.0
LGOS	length of gate-source overlap	mils or microns	LGO	0.0
DE	drain effect factor (short channel parameter)	-	0.0	0.2
GAMMA	velocity saturation factor (short channel parameter)	-	0.0	0.2
MS	sidewall grading coefficient	-	0.33	0.33
TPOLY	fringing capacitance parameter	mils or microns	0.0	0.0
MIL	keyword indicating the dimensions are in mils.			
MICRON	keyword indicating the dimensions are in microns.			

A.8. Subcircuits

A subcircuit that consists of SLATE elements can be defined and referenced in a fashion similar to device models. The subcircuit is defined in the input deck by a grouping of element cards; the program then automatically inserts the group of elements wherever the subcircuit is referenced. Subcircuits have a very important usage in SLATE. The node tearing algorithm [5], used in SLATE to exploit latency, uses the subcircuits defined by the user as subnetworks which can be left out of the analysis if they are not active, i.e., latent. This ability is what makes SLATE different from other commonly used simulators, and provides savings in computer execution time. Therefore, to take advantage of the latency scheme in SLATE, the user must partition the network into subnetworks using the subcircuit command. An example of subcircuit usage is given at the end of this APPENDIX (sec. A.10).

A.8.1. SUBCKT card

General form

```
.SUBCKT subnam N1 <N2 N3 ...>
```

Examples:

```
.SUBCKT NAND2 10 20 30 40
```

A circuit definition is begun with a .SUBCKT card. SUBNAM is the subcircuit name, and N1, N2, ... are the external nodes, which cannot be zero. The group of element cards which immediately follow the .SUBCKT card define the subcircuit. The last card in a subcircuit definition is the .ENDS card (see below). Control and device model cards may not

appear within a subcircuit definition; however, subcircuit definitions may contain anything else, including other subcircuit definitions and subcircuit calls (see below). Note that any subcircuit definitions included as part of a subcircuit definition are strictly local (i.e., such definitions are not known outside the subcircuit definition). Also, any element nodes not included on the .SUBCKT card are strictly local, with the exception of 0 (ground) which is always global.

A.8.2. ENDS card

General form

.ENDS <SUBNAM>

Examples:

.ENDS NAND2

This card must be the last one for any subcircuit definition. The subcircuit name, if included, indicates which subcircuit definition is being terminated; if omitted, all subcircuits being defined are terminated. The name is needed only when nested subcircuit definitions are being made.

A.8.3. Subcircuit calls

General form

XYYYYYYY N1 <N2 N3 ...> SUBNAM

Examples:

X1 1 2 3 4 NAND2

Subcircuits are used in SLATE by specifying pseudo-elements beginning with the letter X, followed by the circuit nodes to be used in expanding the subcircuit.

A.9. Control Cards

A.9.1. TEMP card

General form

.TEMP T1 <T2 <T3 ...>>

Examples:

.TEMP -65.0 25.0 115.0

This card specifies the temperatures at which the circuit is to be simulated. T1, T2, ... are the different temperatures, in degrees C. Temperatures less than -223.0 deg C are ignored. Model data are specified at TNOM degrees (see the .OPTIONS card for TNOM); if the .TEMP card is omitted, the simulation will also be performed at a temperature equal to TNOM.

A.9.2. WIDTH card

General form

.WIDTH IN=COLNUM OUT=COLNUM

Examples:

.WIDTH IN=72 OUT=133

COLNUM is the last column read from each line of input; the setting takes effect with the next line read. The default value for COLNUM is 80. The out parameter specifies the output print width.

Permissible values for the output print width are 80 and 133.

A.9.3. OPTIONS card

General form

.OPTIONS OPT1 OPT2 ... (or OPT=OPTVAL ...)

Examples:

.OPTIONS NOACCT NOLIST NONODE

This card allows the user to reset program control and user options for specific simulation purposes. Any combination of the options listed in the Table A.5 may be included, in any order. 'x' (below) represents some positive number.

Table A.5 Options Listing

OPTION	EFFECT
NOACCT	suppresses the printout of accounting and run time statistics.
NOLIST	suppresses the printout of the summary listing of the input data.
NOMOD	suppresses the printout of the model parameters.
NONODE	suppresses the printing of the node table.
NOOPTS	suppresses the printing of option values.
GMIN=x	resets the value of GMIN, the minimum conductance allowed by the program. The default value is 1.0E-12.
RELTOL=x	resets the relative error tolerance of the program. The default value is 0.001 (0.1 percent).
ABSTOL=x	resets the absolute current error tolerance of the program. The default value is 1 picoamp.
VNTOL=x	resets the absolute voltage error tolerance of the program. The default value is 1 microvolt.
TRTOL=x	resets the transient error tolerance. The default value is 7.0. This parameter is an estimate of the factor by which SLATE overestimates the actual truncation error.

Table A.5 (cont.)

CHGTOL=x	resets the charge tolerance of the program. The default value is 1.0E-14.
NUMDGT=x	resets the number of significant digits printed for output variable values. X must satisfy the relation $0 < x < 8$. The default value is 4. Note: this option is independent of the error tolerance used by SLATE (i.e., if the values of options RELTOL, ABSTOL, etc., are not changed then one may be printing numerical 'noise' for NUMDGT > 4.
TNOM=x	resets the nominal temperature. The default value is 27 deg C (300 deg K).
ITL1=x	resets the dc iteration limit. The default is 150.
ITL2=x	resets the dc transfer curve iteration limit. The default is 30.
ITL4=x	resets the transient analysis timepoint iteration limit. The default is 50.
ITL5=x	resets the transient analysis total iteration limit. The default is 10000. Set ITL5=0 to omit this test.
CPTIME=x	the maximum cpu-time in seconds allowed for this job.
LIMTIM=x	resets the amount of cpu time reserved by SLATE for generating plots should a cpu time-limit cause job termination. The default value is 2 (seconds).
LIMPTS=x	resets the total number of points that can be printed or plotted in a dc, ac, or transient analysis. The default value is 1001.
LVLTIM=x	if x is 1 (one), the iteration timestep control is used. if x is 2 (two), the truncation-error timestep is used. The default value is 2. If method=Gear and MAXORD>2 then LVLTIM is set to 2 by SLATE.
METHOD=name	sets the numerical integration method used by SLATE. Possible names are Gear or trapezoidal. The default is trapezoidal.
MAXORD=x	sets the maximum order for the integration method if Gear's variable-order method is used. X must be between 2 and 6. The default value is 2.

A.9.4. OP card

General form

.OP

The inclusion of this card in an input deck will force SLATE to determine the dc operating point of the circuit with capacitors opened and inductors shorted. Note: a dc analysis is automatically performed prior to a transient analysis to determine the transient initial conditions. SLATE performs a dc operating point analysis if no other analyses are requested.

A.9.5. DC card

General form

.DC SRCNAM VSTART VSTOP VINCR

Examples:

```
.DC VIN 0 5 .2
.DC VDS 0 5 .5
.DC IB  0 10U 1U
```

This card defines the dc transfer curve source and sweep limits. SRCNAM is the name of an independent voltage or current source. VSTART, VSTOP, and VINCR are the starting, final, and incrementing values respectively. The first example will cause the value of the voltage source VIN to be swept from 0.0 volts to 5.0 volts in increments of 0.2 volts.

A.9.6. INITIAL card

General form

```
.INITIAL NODNUM=VAL NODNUM=VAL ...
```

Examples:

```
.INITIAL 12=4.8 4=0.20
```

This card helps the program find the dc or initial transient solution by making a preliminary pass with the specified nodes held to the given voltages. The restriction is then released and the iteration continues to the true solution. The .INITIAL card may be necessary for convergence on bistable or astable circuits. In general, this card should not be necessary.

A.9.7. FORCE card

General form

```
.FORCE NODNUM=VAL NODNUM=VAL ...
```

Examples:

```
.FORCE 2=5.0 3=0.0
```

This card forces the circuit to converge to the specified node voltages. The .FORCE card may be used to force regenerative switching circuits or circuits with positive feedback to a desired state. This card is different from .INITIAL card in that no more iterations are made once the circuit converges to the specified state. In general, this card should not be necessary.

A.9.8. TRAN card

General form

.TRAN TSTEP TSTOP ⟨TSTART ⟨TMAX⟩⟩ ⟨UIC⟩

Examples:

.TRAN 1NS 100NS

.TRAN 1NS 1000NS 500NS

.TRAN 10NS 1US UIC

TSTEP is the printing or plotting increment for line-printer output. For use with the post-processor, TSTEP is the suggested computing increment. TSTOP is the final time, and TSTART is the initial time. If TSTART is omitted, it is assumed to be zero. The transient analysis always begins at time zero. In the interval ⟨zero, TSTART⟩, the circuit is analyzed (to reach a steady state), but no outputs are stored. In the interval ⟨TSTART, TSTOP⟩, the circuit is analyzed and outputs are stored. TMAX is the maximum stepsize that SLATE will use (for default, the program chooses 2*TSTEP). TMAX is useful when one wishes to guarantee a computing interval which is smaller than twice the print interval.

UIC (use initial conditions) is an optional keyword which indicates that the user does not want SLATE to solve for the quiescent operating point before beginning the transient analysis. If this keyword is specified, SLATE uses the values specified using IC=... on the various elements as the initial transient condition and proceeds with the analysis.

A.9.9. PRINT cards

General form

.PRINT PRTYPE OV1 <OV2 ... OV8>

Examples:

.PRINT TRAN V(4) I(VIN)

.PRINT DC V(5) I(VOUT) V(8,9)

This card defines the contents of a tabular listing of one to eight output variables. PRTYPE is the type of the analysis (DC or TRAN) for which the specified outputs are desired. The form for voltage or current output variables is as follows:

V(N1<,N2>) specifies the voltage difference between nodes N1 and N2. If N2 (and the preceding comma) is omitted, ground (0) is assumed.

I(VXXXXXXX) specifies the current flowing in the independent voltage source named VXXXXXXX. Positive current flows from the positive node, through the source, to the negative node. There is no limit on the number of .PRINT cards for each type of analysis.

A.9.10. PLOT cards

General form

.PLOT PLTYPE OV1 <(PLO1,PHI1)> <OV2 <(PLO2,PHI2)> ... OV8>

Examples:

.PLOT DC V(4) V(5) V(1)

.PLOT TRAN V(7,5) (0,5) I(VIN) V(7) (1,9)

This card defines the contents of one plot of from one to eight output variables. PLTYPE is the type of analysis (DC or TRAN) for which the specified outputs are desired. The syntax for the OVI is identical to that for the .PRINT card, described above.

The optional plot limits (PLO,PHI) may be specified after any of the output variables. All output variables to the left of a pair of plot limits (PLO,PHI) will be plotted using the same lower and upper plot bounds. If plot limits are not specified, SLATE will automatically determine the minimum and maximum values of all output variables being plotted and scale the plot to fit. More than one scale will be used if the output variable values warrant (i.e., mixing output variables with values which are orders-of-magnitude different still gives readable plots). The overlap of two or more traces on any plot is indicated by the letter X.

When more than one output variable appears on the same plot, the first variable specified will be printed as well as plotted. If a printout of all variables is desired, then a companion .PRINT card should be included. There is no limit on the number of .PLOT cards specified for each type of analysis.

A.10. Example Input Decks

This section list some example input decks for SLATE.

Example 1:

The first example cumputes the dc transfer curve of a bipolar TTL inverter.

```
Biploar TTL inverter transfer curve
* input node(1) output node(8)
r1 9 2 4k
r2 4 0 1k
r3 9 5 1.4k
r4 9 6 100
q1 3 2 1 bjp
q2 5 3 4 bjp
q3 6 5 7 bjp
q4 8 4 0 bjp
d1 7 8 diode
v1 1 0 dc
vdd 9 0 5
.model bjp npn(bf=100 br=0.1 rc=10 rb=10 re=5 va=200 nc=1 ne=1)
.model diode d(rs=10)
.dc v1 0 5 0.2
.plot dc v(8)
.end
```

Example 2:

This example lists the input deck used in example 3.1 in Chapter 3. The circuit is a chain of NMOS inverters.

```
This is a circuit to test latency scheme in slate
.subckt inverter 1 2 3
*** nodes: vdd output input
m1 1 3 3 0 dm w=5 l=10 as=25 ad=25 ass=15 asd=50
+             rdd=35 rss=35 cgs=1.725f cgd=1.725f
m2 3 2 0 0 em w=10 l=5 as=100 ad=100 ass=40 asd=35
+             rdd=35 rss=35 cgs=3.45f cgd=3.45f
.ends
vdd 1 0 5
vin 2 0 pulse(0 5 1n 1n 1n 75n 152n)
* A chain of 10 inverters
x1  1 2  3  inverter
x2  1 3  4  inverter
x3  1 4  5  inverter
x4  1 5  6  inverter
x5  1 6  7  inverter
x6  1 7  8  inverter
x7  1 8  9  inverter
x8  1 9  10 inverter
x9  1 10 11 inverter
x10 1 11 12 inverter
.model dm nmos vto=-2 kp=10u be=0.52 lambda=0.05 kpn=.0918f
+             ms=0.33 cox=.345f theta=1e-20 micron
```

```
.model em nmos vto=1 kp=10u be=0.52 lambda=0.05 kpn=.0918f
+              ms=0.33 cox=.345f theta=1e-20 micron
.options abstol=1.0e-12 vntol=1e-6 reltol=1e-3
.tran 1n,76n
.print tran v(1) v(2) v(3) v(4) v(5) v(6) v(7) v(8)
.print tran v(9) v(10) v(11) v(12)
.plot tran v(1) v(2) v(3) v(4) v(5) v(6) v(7) v(8)
.plot tran v(9) v(10) v(11) v(12)
.end
```

Example 3:

This example shows the use of the subcircuits in SLATE. The circuit is a NMOS one bit full adder. This input deck was used in example 3.2 in Chapter 3.

```
 one bit full adder circuit
 *inverter
.subckt inv 10 20 30
 *** nodes:  vdd  output  input
 m1 10 20 20 0 dm w=5 l=10
 +             as=25 ad=25 ass=15 asd=20 cgs=1.725f cgd=1.725f
 +             rdd=35 rss=35
 m2 20 30 0  0 em w=10 l=5
 +             as=100 ad=100 ass=40 asd=35 cgs=3.45f cgd=3.45f
 +             rdd=35 rss=35
.ends
 *2-input nand
.subckt nand2 10 40 50 60
 *** nodes:  vdd  output  input(2)
 m1 10 40 40 0 dm w=5 l=20
 +             as=25 ad=25 ass=15 asd=20 cgs=1.725f cgd=1.725f
 +             rdd=35 rss=35
 m2 40 50 55 0 em w=10 l=5
 +             as=50 ad=100 ass=20 asd=35 cgs=3.45f cgd=3.45f
 +             rdd=35 rss=35
 m3 55 60 0  0 em w=10 l=5
 +             as=100 ad=50 ass=40 asd=20 cgs=3.45f cgd=3.45f
 +             rdd=35 rss=35
.ends
 *3-input nand
.subckt nand3 10 70 80 90 100
 *** nodes:  vdd  output  input(3)
 m1 10 70 70 0 dm w=5 l=20
 +             as=25 ad=25 ass=15 asd=20 cgs=1.725f cgd=1.725f
```

```
+              rdd=35 rss=35
m2 70 80 75 0 em w=15 l=5
+              as=75 ad=150 ass=20 asd=45 cgs=5.175f cgd=5.175f
+              rdd=35 rss=35
m3 75 90 85 0 em w=15 l=5
+              as=75 ad=75 ass=20 asd=20 cgs=5.175f cgd=5.175f
+              rdd=35 rss=35
m4 85 100 0 0 em w=15 l=5
+              as=150 ad=75 ass=45 asd=20 cgs=5.175f cgd=5.175f
+              rdd=35 rss=35
.ends
*4-input nand
.subckt nand4 10 110 120 130 140 150
*** nodes:  vdd  output  input(4)
m1 10  110 110 0 dm w=5 l=20
+              as=25 ad=25 ass=15 asd=20 cgs=1.725f cgd=1.725f
+              rdd=35 rss=35
m2 110 120 115 0 em w=20 l=5
+              as=100 ad=200 ass=30 asd=55 cgs=6.9f cgd=6.9f
+              rdd=35 rss=35
m3 115 130 125 0 em w=20 l=5
+              as=100 ad=100 ass=30 asd=30 cgs=6.9f cgd=6.9f
+              rdd=35 rss=35
m4 125 140 135 0 em w=20 l=5
+              as=100 ad=100 ass=30 asd=30 cgs=6.9f cgd=6.9f
+              rdd=35 rss=35
m5 135 150 0   0 em w=20 l=5
+              as=200 ad=100 ass=60 asd=35 cgs=6.9f cgd=6.9f
+              rdd=35 rss=35
.ends
* nominal circuit
vdd 10 0 5
vc1 1  0 pulse(0 5 0 2n 2n 125n 254n)
va0 2  0 pulse(0 5 0 2n 2n 125n 254n)
vb0 3  0 pulse(0 5 0 2n 2n 125n 254n)
x1  10 12 1  11       nand2
x2  10 13 2  11       nand2
x3  10 14 3  11       nand2
x4  10 15 1  2  3     nand3
x5  10 16 12 13 14 15 nand4
x6  10 6  1  2        nand2
x7  10 7  1  3        nand2
x8  10 8  2  3        nand2
x9  10 9  6  7  8     nand3
x10 10 11 9           inv
.print tran v(1) v(2) v(3) v(9) v(16)
.plot tran v(1) v(2) v(3) v(9) v(16)  (0,5)
.model dm nmos vto=-2 kp=10u be=0.52 lambda=0.05 kpn=.0918f
+              ms=0.33 cox=.345f theta=1e-20 micron
.model em nmos vto=1 kp=10u be=0.52 lambda=0.05 kpn=.0918f
+              ms=0.33 cox=.345f theta=1e-20 micron
```

```
.tran 1n,125n
.end
```

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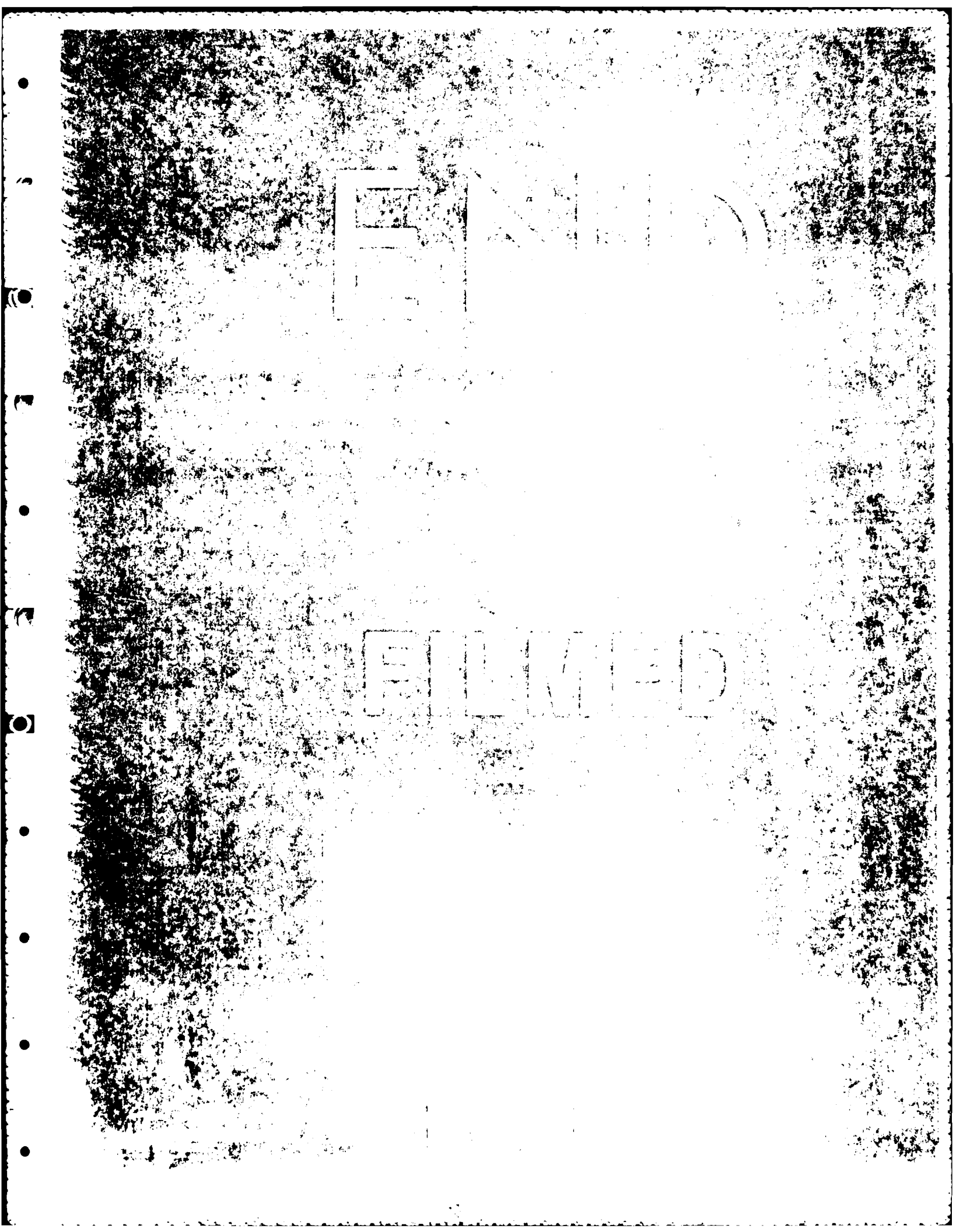
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